ANALYSIS OF S-BAND SOLID-STATE TRANSMITTERS FOR THE SOLAR POWER SATELLITE

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PREFACE

This report describes the findings of a short (7-month) preliminary study of the feasibility of using a solid-state transmitter for the Solar Power Satellite. The study was performed in the Microwave Technology Center of RCA Laboratories. The Center's director is Fred Sterzer. Markus Nowogrodzki was Program Manager for the study. The contributing scientists were Erwin F. Belohoubek, Morris Ettenberg, Ho C. Huang, and Franco N. Sechi.

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I. INTRODUCTION

This report describes the finding of a short (7-month) preliminary study of the applicability of solid-state transmitter modules to the Solar Power Satellite concept and the effect such an approach may have on the projected system. The program called for the development of background information so that subsequent detailed tradeoff analyses of the various system elements could be performed. The study was concerned with three distinct but interrelated areas: the overall system concepts, the characteristics of the transmitter modules, and the active solid-state devices used in the modules.

The basis for the study was the Reference System SPS as defined by the Department of Energy (DOE) and the National Aeronautics and Space Administration (NASA) in the Reference System Report of October, 1978. Thus, the fundamental characteristics of the system -- such as the transmitted microwave-beam frequency of 2.45 GHz, the basic efficiency assignment for the system elements, and the maximum allowed power density in the ionosphere -- were accepted as basic tenets for the study.

The methodology of the study was as follows: In the first phase, the system, module, and device investigations were pursued independently of one another, the only guiding concept being general adherence to the ideas developed for the microwave tube-based transmitter. This line of investigation was at the specific request of the NASA technical monitoring activity, since it was desired to assess the feasibility of simply replacing the microwave thermionic transmitting devices with clusters of solid-state device elements. As described in this study, this approach proved technically imprudent -- for different reasons. An alternate approach -- a proprietary RCA concept proposed for various other large spaceborne structures -- in which a solar-cell "blanket" is used to provide dc power to a distributed array of solid-state amplifiers whose output power is combined in space -- was then analyzed, still maintaining the general constraints of the Reference System. Devices and modules suitable for this approach were studied, and preliminary designs suitable for further investigations were developed.

The driving force behind the study was the realization that the technology of microwave solid-state devices has reached the point where basic feasibility of replacing thermionic transmitters could be postulated, with the attendant benefits to the ultimate system, notably greatly enhanced reliability and graceful degradation of the transmitter. The major unknown of a solid-state transmitter approach is the possibility of attaining the required power-added efficiency in the power amplifiers by the use of solid-state devices, particularly gallium arsenide FETs, which offer the prospect of simplicity of design in future mass production schemes. It was therefore judged important to include in the program measurements on an actual FET power stage at the SPS frequency, even though such a task was not part of the original Statement of Work. The results of this measurement, which have proved quite encouraging, are included in this report, and the amplifier will be delivered to NASA as part of the effort on this program.

The concept of a solid-state SPS transmitter takes on particular significance in light of the latest findings concerning GaAs FET reliability, studied by RCA under concurrent programs. The reliability tests are run on amplifier stages providing about 4 W of output power at 4 GHz, with device channel temperatures maintained at 200°C. (The criterion for "failure" used in these tests is a reduction in amplifier power output by 0.5 dB.) On the basis of information accumulated to date, GaAs power FETs are predicted to have a failure rate of 150 FITs (1 FIT = 1 failure per 10^9 device hours), which translates into a probability of device survival in 30 years of the order of 95%. Perhaps of even greater importance, these life tests are providing important information on the causes of failures in FETs, so that we believe that we are already in a position to design devices having even higher reliability.

II. SYSTEM STUDIES

A. INTRODUCTION

This study uses as a basis the Reference System SPS as defined by DOE and NASA in the Reference System Report of October, 1978. The implications of the replacement of the klystron transmitter by a solid-state transmitter are considered. This leads to the conclusion that the direct replacement entails an unacceptable weight penalty due to (1) the thermal control system required for the solid-state device substrate; (2) the low-voltage/high-current power distribution and conditioning system; and (3) the degradation of efficiency due to microwave power combiners required for high-power modules.

An alternative system, based on an RCA concept proposed for many different large structures in space, is considered. In this approach, a "blanket" of solar cells provides power directly to relatively small clusters of microwave amplifier modules having only moderate power output. The major problems of the klystron-replacement system, namely those of loss of efficiency due to power combining, losses in the voltage distribution system, and thermal difficulties, are completely eliminated in such a system. A new complication is, however, introduced, since the system requires different orientations of the solar blanket (facing the sun) and the microwave array (facing the rectenna); large mirrors in space are therefore required. The acronym SMART (Solar Microwave Array Technology) is RCA's designation of the system.

B. THE REFERENCE SYSTEM DESIGN

We consider the simplified efficiency chain adopted from the Reference System as shown in Fig. II.1.

Some of the numerical parameters of the system are shown in Fig. II.2.

The reference system may be designed on the basis of the analysis by Goubau [1] who finds, for maximum transmission efficiency, that the transmitter antenna should be fed with a Gaussian taper and a quadratic phase shift.

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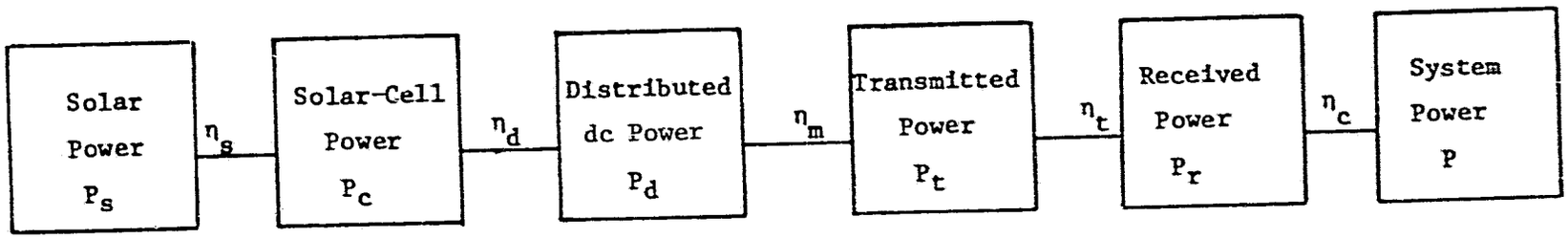
1. G. Goubau, "Microwave Power Transmission from an Orbiting Solar Power Station," J. Microwave Power 5, 4 (1970).



η_s = Solar-Cell Conversion Efficiency
η_d = Power Distribution and Conditioning Efficiency
η_m = Microwave Conversion and Combination Efficiency
η_t = Transmission Efficiency
η_c = Rectenna Conversion Efficiency
D_t = Transmitting-Antenna Diameter
D_r = Rectenna Diameter

Figure II.1. SPS Reference System simplified efficiency chain.

PHYSICAL PARAMETERS

SOLAR CONSTANT (AVERAGE)	S_o	1350	W/m^2
MICROWAVE FREQUENCY	f	2.45	GHz
MICROWAVE WAVELENGTH	λ	0.1224	m
DISTANCE TO GEOSTATIONARY ORBIT	R	35,786	km

CONVENIENT APPROXIMATIONS

RAYLEIGH DISTANCE PARAMETER	$2\lambda R = 8.76\ m \times 10^6\ m$	$\cong$	$9 \times 10^6\ m^2$
WAVELENGTH SQUARED	$\lambda^2 = 1.498\ m \times 10^{-2}\ m$	$\cong$	$150\ cm^2$
SOLAR-CELL EFFICIENCY (INCL. DEGRADATION)	$\eta_s = 0.13$	=	13%
TRANSMISSION EFFICIENCY (INCL. ATMOSPHERICS)	$\eta_t = 0.87$	=	87%
RECTENNA EFFICIENCY	$\eta_c = 0.85$	=	85%
TEMPERATURE OF RADIATION-COOLED SOLAR PANEL	$T_s = 330\ K$	=	57°C
MAXIMUM ALLOWED POWER DENSITY (IONOSPHERE)	$P_{ro} = 230\ mW/m^2$	=	$23\ mW/cm^2$

Figure II.2. SPS numerical parameters.

$$E_t(\rho) = E_{to} \exp -\frac{1}{2} \alpha \frac{2\rho^2}{D_t} \exp j \frac{\pi}{\lambda D_t} \rho^2 \qquad (1)$$

The product of the transmitting and receiving antennas is constrained by the requirement

$$D_r D_t \geq 2\lambda R \qquad (2)$$

For a minimal size system we have

$$D_r D_t = 8.76 \text{ m} \times 10^6 \text{ m} \simeq 9 \text{ km}^2$$

In this design, the receiving antenna pattern is also a 10-dB Gaussian taper with total power,

$$P_r = 0.31 \, p_{ro} \, D_r^2 \qquad (3)$$

A nomograph, which may be used for system design, is shown in Fig. II.3. This nomograph for system power assumes a transmission efficiency $\eta_t = 87\%$ and a rectenna efficiency $\eta_c = 85\%$.

The lines marked (A), (B), and (C) correspond to Eqs. (1), (2), and (3) for the Reference System. Line (C) is determined by the maximum peak received power density of 23 mW/cm^2 and a system power of 5000 MW. This determines the rectenna diameter of 9.3 km.

Line (B) is now drawn through the rectenna diameter and the transmission efficiency $\eta_t = 87\%$ to determine the diameter of the transmitting antenna $D_t = 0.95$ km. Using $D_t = 1$ and the system power $P = 5000$, we draw line (A), which determines the peak transmitting antenna power density $p_{to} = 21$ kW/m^2. For device considerations, the latter quantity is also given in terms of watts per square wavelength as $P_{mo} = 350$ W. Since this is a 10-dB taper design, the power density at the outer rim of the rectenna is 2.3 mW/cm^2, and the required transmitter module per square wavelength at the transmitter antenna rim is 35 W.

Since the peak received power density is limited to 23 mW/cm^2 due to presumed local overheating effects, we may consider that for reasons of efficiency the system will be designed to work at that level. Based on a

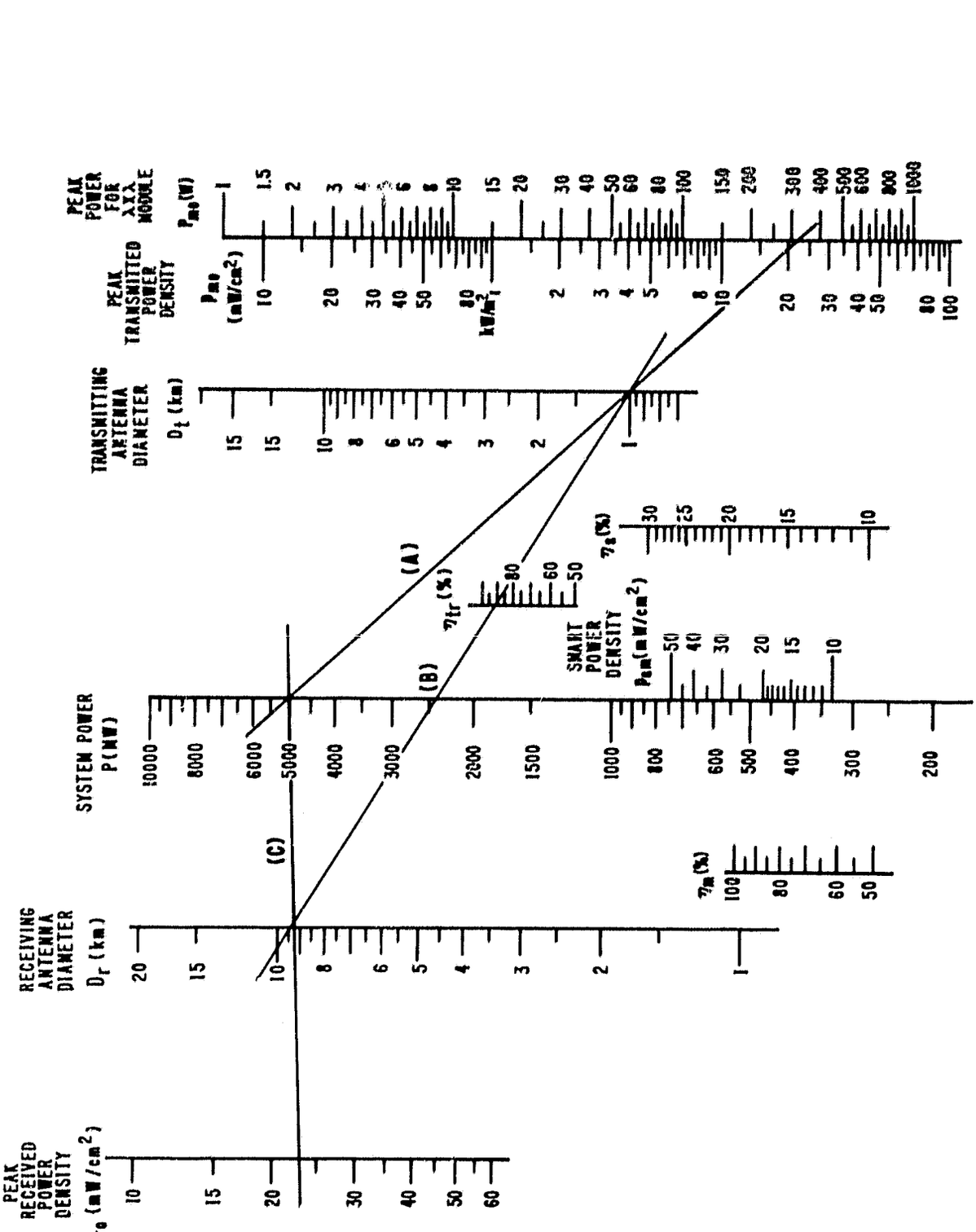


Figure II.3. Nomograph for SPS design (10-dB Gaussian taper).

microwave device and circuit efficiency of $\eta_m = 80\%$, the system design parameters are shown in Fig. II.4. The further assumptions made in Fig. II.4 are solar-cell efficiency $\eta_s = 13\%$ and power distribution efficiency $\eta_d = 90\%$. The substrate temperature of the solid-state circuits is derived from a two-sided radiating surface with emissivity of 1. The quantity L_s represents the length of the side of a square solar array required for the system. Silicon cells with a solar concentration ratio of 1 are used in the array.

The following equations are plotted in Fig. II.4:

$$\begin{aligned}
&\text{System Power:} && P = 265\sqrt{P_m} \quad \text{(MW)} \\
&\text{Transmitter Diameter:} && D_t = \frac{4.13}{\sqrt[4]{P_m}} \quad \text{(km)} \\
&\text{Rectenna Diameter:} && D_r = 2.14\sqrt[4]{P_m} \quad \text{(km)} \\
&\text{Substrate Temperature:} && T_k = 100\sqrt[4]{P_m} \quad \text{(K)} \\
&\text{Solar Panel Side:} && L_s = 1.67\sqrt[4]{P_m} \quad \text{(km)}
\end{aligned} \tag{4}$$

where P_m is the peak module power per squared wavelength.

M_{ts} is the ratio in percent of the transmitter antenna area to the solar-cell area. All quantities are read on the left ordinate scale except M_{ts}, T_k, and P_m.

Two designs taken from Fig. II.4 are shown as examples, and the derived numerical results are given in Table II.1. In addition, a third design, derived from Eq. (4), is shown.

C. REFERENCE SYSTEM USE OF SOLID-STATE DEVICES

1. Temperature

A basic limitation on the use of solid-state devices is the need to keep the device channel or junction temperature to a maximum of 120°C in order to assure long life. It is estimated that the temperature drop from the channel or junction to the substrate will be 80-60°C, limiting the substrate temperature to 40-60°C. By reference to Fig. II.4 or Table II.1, we see that a nominal 2.0-GW system represents a reasonable upper limit for a solid-state system that does not use special cooling.

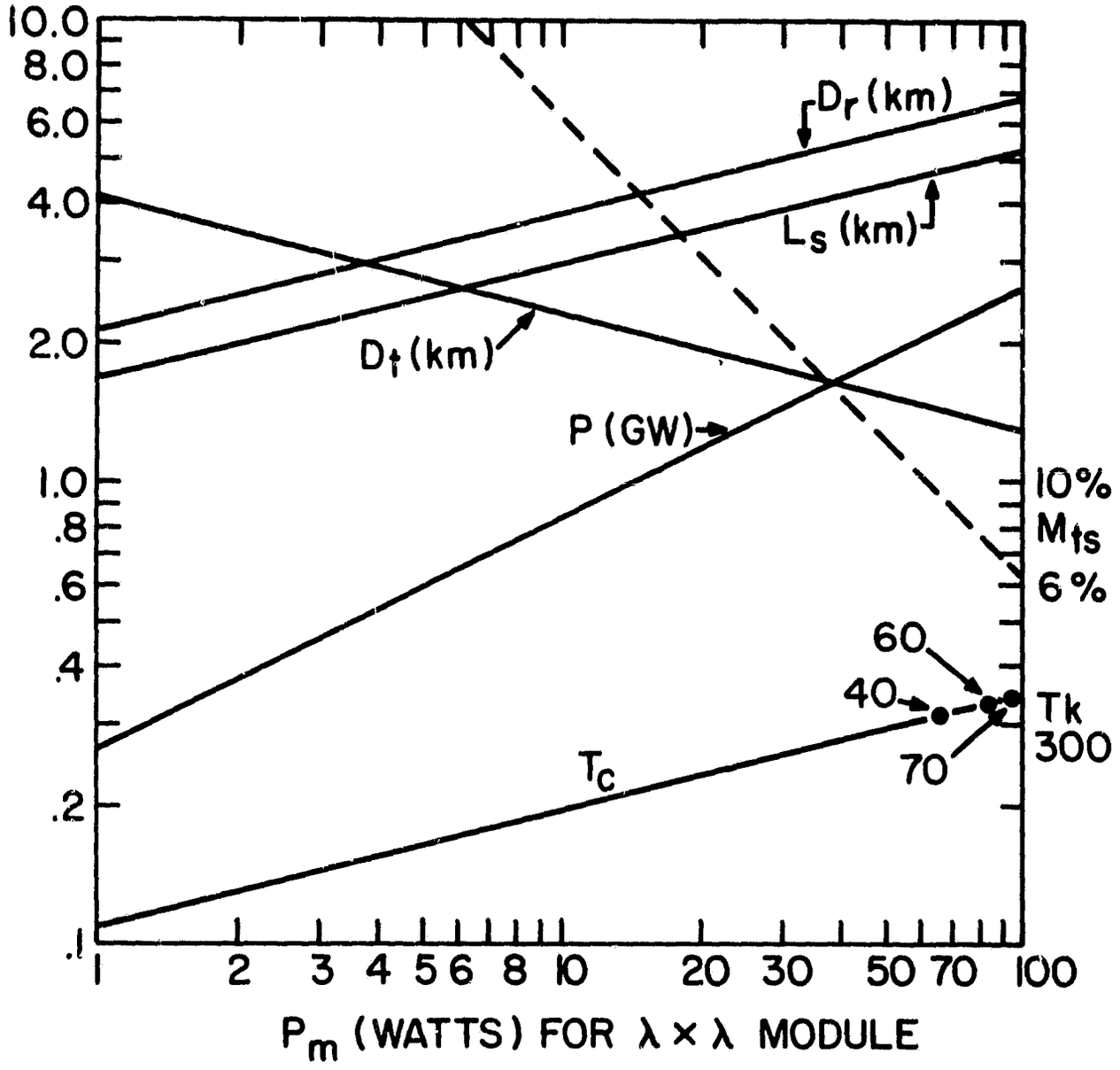


Figure II.4. SPS design (10-dB Gaussian taper).

TABLE II.1. SPS DESIGN (10-dB GAUSSIAN TAPER)

Parameter	Symbol	Unit	Design (1)	Design (2)	Design (3)
System Power	P	MW	1000	2000	5000
Peak Module Power	P_m	w/λ^2	14	57	350
Transmitter Diameter	D_t	km	2.1	1.5	0.95
Rectenna Diameter	D_r	km	4.2	5.9	9.3
Solar Array Side	L_s	km	3.2	4.6	7.25
Substrate Temperature	$T_k(T_c)$	K(°C)	214(-59)	302(29)	478(205)
Area Ratio	M_{ts}	%	34	8	1

2. Voltage Distribution

The klystrons used in the Reference System are high-voltage devices, operating at 40,000 V. The solid-state devices are low-voltage devices operating at 10-20 V, and it may be possible to operate a string of these devices in series at a string voltage of 200 V. The device current would then be increased by a factor of 200. Since the conductor loss is given by $IR = I^2 (\rho \ell/A)$, we see that the cross-sectional area of the power conductor line must be increased by a factor of $(200)^2 = 40{,}000$ to keep the losses the same in the klystron and solid-state cases. This will entail a weight penalty.

A second weight penalty will be incurred in the power conditioning or dc/dc conversion system. In order to reduce the conductor weight it would be preferable to distribute the power at the high voltage (40,000 V) to large panels where it would be transformed to some intermediate voltage (e.g. 2000 V) and then distributed to the string level where it would be converted to 200 V. Here again we incur a weight penalty because of the requirement of a two-pass voltage conversion and distribution system.

3. Microwave Power Combiners

The individual solid-state devices are inherently limited to power on the order of 3-5 W. Therefore, the output power from a large number of devices will have to be combined in order to achieve the required module

power. This will entail reflection and transmission losses in the microwave circuits. Even though each particular combiner may be designed for a loss of only a few tenths of a decibel, the large number of combiners will produce a serious degradation in efficiency with a consequent increase in primary power requirements.

D. COMPARISON OF 5-GW REFERENCE SYSTEM AND 2-GW SOLID-STATE SYSTEM

The mass statement in the Reference System Report has been used to estimate the mass of a 2-GW solid-state system. It should be noted that this is a very crude estimate because it involves many unknowns.

Table II.2 shows the comparative mass statements and the scaling factors used. The notes indicate the further assumptions made in deriving the estimated quantities.

As a figure of merit, the specific power (ratio of total system power to system mass) is compared. The conclusion that we draw from this comparison is that the solid-state replacement falls below the klystron system by 30%.

E. SMART SYSTEMS

Since the direct replacement of klystrons by solid-state devices appears unattractive, we are led to utilize the major advantages of solid-state devices; in other system concepts, these are long life and high reliability. Since the solar cell is itself a solid-state device, we think in terms of structures that integrate the microwave device more closely with the solar cell. To this end we have proposed the application of SMART (Solar Microwave Array Technology) modules to the SPS. SMART modules had originally been proposed for communication satellites and other large space structures.

Instead of using the exponential taper design, which tends to optimize in the direction of smaller, high-power transmitting antennas, we consider uniform microwave power distribution. This analysis of SPS systems is based on the study of parallel or tubular beams by Ramsay [2].

2. J. F. Ramsay, "Tubular Beams from Radiating Apertures," Vol. 3 of Adv. Microwaves (Academic Press Inc., New York, 1968).

TABLE II.2. SPS SYSTEM MASS COMPARISON (KLYSTRON REFERENCE vs SOLID STATE)

Quantity	Unit	Reference System (Klystron)	Scaling Factor	Replacement System (Solid State)
System Parameters				
System Power	MW	5000		2000
Peak Module Power	W/λ^2	350		100
Microwave Efficiency	%	85		57(1)
Transmitter Diameter	km	0.95		1.5
Rectenna Diameter	km	9.30		5.9
Solar-Cell Area	km^2	50.1		30.6
Mass	10^6 kg			
Solar Array				
Solar Cells		22.1	Mass/area	13.5
Structure		3.8	Mass/area	2.3
Power Distribution		1.1	Mass/area/ solar power	0.4
Control		0.3	Mass/mass	0.2
Antenna				
Microwave Circuits		7.2		0.05(2)
Structure		1.1	Mass/area/ dc power	1.6
Power Distribution		2.2	Mass/area/ dc power	4.8(3)
Thermal Control		2.2		0
Control		0.8	Mass/mass	0.4
Total Mass:		40.8		23.3
Specific Power	W/kg	122.5		85.8

Notes: (1) This assumes η_c = 80% reduced by 1.5 dB due to combiner loss.
(2) This assumes 1 kg per module.
(3) This assumes a factor of 1.5 for a 2-pass power conditioning system.

Put very simply, a uniformly illuminated aperture may be focused to maintain its cross section to a distance, known as the Rayleigh distance, given by

$$R_r = \frac{D^2}{2\lambda}$$

For our purposes, focusing means suitable adjustment of the phase shift of the microwave fields across the transmitting aperture. The possible application to SPS derives from the numerical value for the transmitting aperture, i.e., the diameter of the transmitting antenna when the distance from the Earth to the satellite in geostationary orbit is made equal to the Rayleigh distance.

Let R_r = 36,000 km.
Then $D_t^2 = 2\lambda R \cong 9 \times 10^6$ m and $D_t \cong 3$ km.

This tells us that an antenna of diameter 3 km at a frequency of 2.45 GHz, wavelength 12.24 cm, will have a Rayleigh distance equal to 36,000 km, or the distance from Earth to geostationary orbit. Using the average solar constant S_o = 1350 W/m^2, a solar efficiency of 13%, and a microwave efficiency of 80% we find a uniform power density at the antenna of 14 mW/cm^2 and a total radiated power of 992 MW. This beam, when focused at the rectenna, produces a power density on axis of twice the transmitted power density or 28 mW/cm^2. Since this is above the ionosphere limit, we must reduce the solar cell and microwave module density, keeping the same aperture, by a factor of 23/28 or 82%. The transmitted power is now reduced to 815 MW. A rectenna of diameter D_r = 1.22 km, D_t = 3.7 km will collect 84% of the transmitted power or 685 mW, giving a system power of 580 MW, allowing for η_c = 85%.

In order to keep the sunlight directed onto the solar array as the satellite goes around its daily orbit while keeping its microwave aspect directed to Earth, an RCA proprietary design provides for two mirrors, one fixed and one rotating at 45° to the satellite. Each mirror area is thus twice

the area of the transmitter array. However, these large mirror structures are made of a very light material, e.g., aluminized Kapton* (12.5 μm) with a mass of 0.018 kg/m^2.

A comparison of the Reference System and a SMART system is shown in Table II.3. This rough estimate indicates that a SMART system has a specific power of 10% above the klystron Reference System.

Further consideration of uniform apertures does not show any *a priori* reasons why the SMART System aperture cannot be made larger. As the antenna diameter is increased, the distance from satellite to Earth becomes smaller than the Rayleigh distance, and the field pattern at the rectenna must be calculated by near-field instead of far-field approximations. The general effect of the near-field reception is to lower the power density at the center and increase the power density across the beamwidth. This means that a larger transmitting antenna does not require a smaller receiving antenna.

Since the larger SMART systems have the same power density as the small systems, the specific power as a figure of merit should remain constant since all the parameters scale directly with area. Two designs for large SMART systems are shown in Table II.4.

The power density at the rectenna for the large SMART system is shown in Fig. II.5 as a function of radial distance from the bore sight axis, assuming normal incidence. For comparison, the same parameters for the Reference System are also shown.

F. NUMERICAL CALCULATIONS OF SMART SYSTEMS

To obtain a more accurate estimate of SMART system performance, the radiation pattern was programmed and calculated numerically. Neither far-field nor near-field approximations are made in this program; the only approximation made is that the transmitter antenna diameter and the receiver antenna diameter each be much smaller than the Earth-to-satellite distance.

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*E. I. du Pont de Nemours & Co., Inc., Wilmington, DE.

TABLE II.3. SPS SYSTEM MASS COMPARISON (KLYSTRON REFERENCE vs SMART)

Quantity	Unit	Reference (Klystron)	Scaling Factor	SMART System
System Parameters				
System Power	MW	5000		580
Peak Module Power	W/λ^2	350		1.73
Microwave Efficiency	%	85		80
Transmitter Diameter	km	0.95		3.0
Rectenna Diameter	km	9.3		3.7
Solar Cell Area	km^2	50.1		5.8
Reflector Area	km^2	0		28.4
Mass	10^6 kg			
Solar Array				
Solar Cells		22.1	Mass/area	2.6
Microwave Circuits		0		0.04(1)
Structure		3.8	Mass/area	0.4
Power Distribution		1.1		0
Control		0.3	Mass/mass	0.03
Antenna/Reflector				
Microwave Circuits		7.2		0
Structure		1.1		1.0(2)
Power Distribution		2.2		0
Thermal Control		2.2		0
Control		0.8	Mass/mass	0.1
Total Mass:		40.8		4.2
Specific Power	W/kg	122.5		138.6

Notes: (1) This is based on a 3-W module on a 1.3 λ x 1.3 λ spacing and 1 g per module.
(2) This assumes a 12.5-μm Kapton at 0.018 kg/m^2 and an equal mass of supporting structure.

TABLE II.4. SPS DESIGNS (SMART)

Parameter	Symbol	Unit	SMART Small	SMART Medium	SMART Large
System Power	P	MW	580	2380	5000
Module Power	P_m	w/λ^2	1.73	1.73	1.73
Transmitter Diameter(1)	D_t	km	3.0	6.0	8.5
Rectenna Diameter	D_r	km	3.7	6.0	8.5
Transmission Efficiency	η_t	%	84	86	90
Reflector Area		km^2	28.4	113.6	228.0

NOTE (1): Solar array diameter is the same as transmitter diameter.

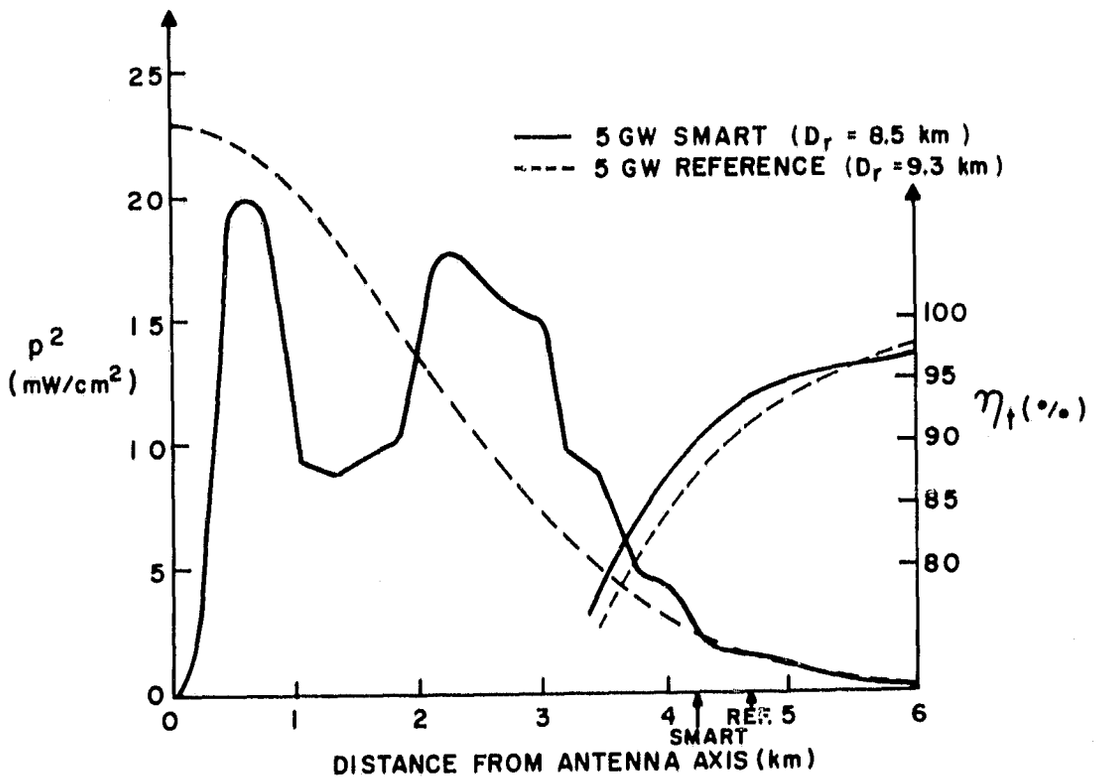

Figure II.5. Power density for the large SMART system.

We assume a uniform power distribution in the SMART antenna and a phase variation proportional to the square of the radius.

In Figs. II.6 through II.8 we show several typical calculations for a 7.8-GW SMART system. The phase shift shown is the total phase shift at the edge of the circular antenna as compared with the signal phase at the center. The table and the graph show the power density at the rectenna as a function of radial distance from the rectenna axis. The efficiency calculation gives the ratio of the power received by the rectenna area of the given radius to the total radiated power.

A comparison of the three power density patterns shows the effects of applying a phase shift of +22.5° as compared with a uniform-phase antenna. The +22.5° phase shift has the effect of pinching in the beam somewhat and producing higher peaks. The -22.5° case shows lower peaks and a broader pattern. The relative beamwidth may be judged from the efficiency at the same diameter, e.g., at 4.0-km radius (8.0-km rectenna diameter). The uniform-phase antenna gives an efficiency of 86.66%, the +22.5° antenna gives 88.08%, and the -22.5° antenna gives 85.07% into the same 8.0-km rectenna.

The same programming technique may be used to calculate antennas having nonuniform power-density distributions and different phase variations.

SYSTEM PARAMETERS:

SOLAR CONSTANT	1358.	WATTS/SQ.METER
SOLAR CELL EFFICIENCY	13.	PER CENT
TRANSMISSION EFFICIENCY	98.	PER CENT
MICROWAVE FREQUENCY	2.45	GIGAHERTZ
MICROWAVE EFFICIENCY	80.	PER CENT
RANGE	35786.	KILOMETERS
PHASE SHIFT	.00	DEGREES
SMART ANTENNA DIAMETER	8.50	KILOMETERS
TRANSMITTED POWER	7807.65	MEGAWATTS

RADIUS KILOMETERS	POWER DENSITY MILLIW/SQ.CM	EFFICIENCY PER CENT	RADIUS KILOMETERS	POWER DENSITY MILLIW/SQ.CM	EFFICIENCY PER CENT
.10	2.01	.02	2.00	20.27	45.29
.20	2.91	.06	2.10	21.17	49.69
.30	6.77	.23	2.20	20.05	54.41
.40	13.67	.67	2.30	17.19	58.42
.50	20.87	1.51	3.00	14.40	61.90
.60	24.77	2.70	3.10	13.10	65.17
.70	23.77	4.04	3.20	13.03	68.52
.80	19.70	5.31	3.30	12.71	71.90
.90	15.62	6.44	3.40	11.16	74.95
1.00	13.48	7.53	3.50	8.81	77.43
1.10	13.07	8.68	3.60	6.98	79.45
1.20	13.03	9.94	3.70	6.33	81.34
1.30	12.46	11.24	3.80	6.32	83.27
1.40	11.41	12.53	3.90	5.91	85.23
1.50	10.29	13.77	4.00	4.78	86.66
1.60	9.45	14.99	4.10	3.50	87.82
1.70	9.29	16.26	4.20	2.82	88.77
1.80	10.47	17.78	4.30	2.81	89.75
1.90	13.40	19.82	4.40	2.86	90.76
2.00	17.34	22.02	4.60	2.48	91.65
2.10	20.51	26.08	4.60	1.79	92.32
2.20	21.40	29.87	4.70	1.29	92.80
2.30	20.25	33.61	4.80	1.22	93.27
2.40	18.83	37.25	4.90	1.00	93.60
2.50	18.89	41.00	5.00	1.30	94.03

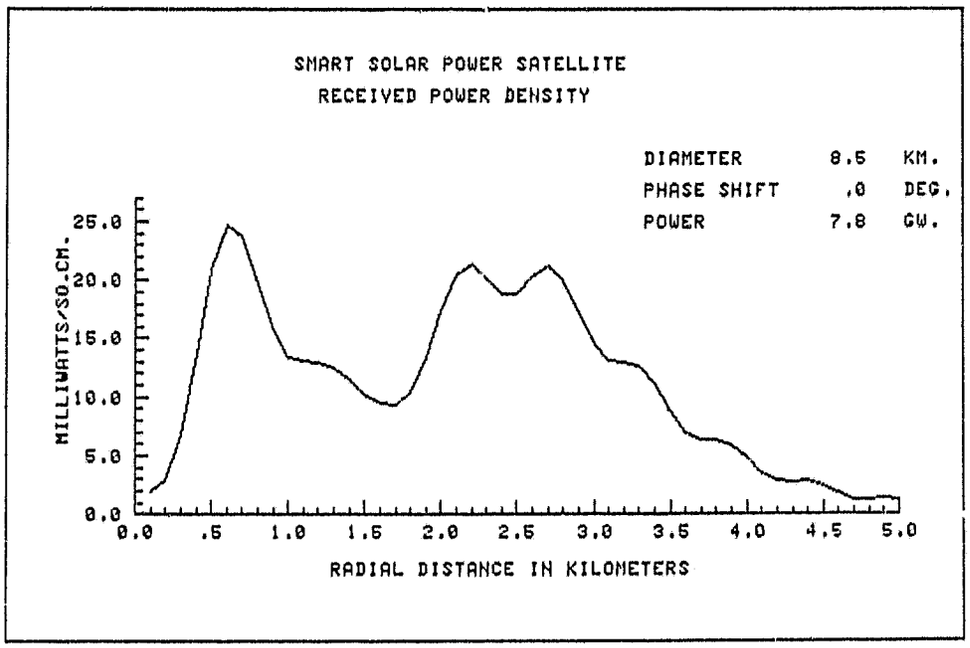

Figure II.6. SMART Solar Power Satellite - radiation calculation (phase shift = 0°).

SYSTEM PARAMETERS:

SOLAR CONSTANT	1360.	WATTS/SQ.METER
SOLAR CELL EFFICIENCY	13.	PER CENT
TRANSMISSION EFFICIENCY	90.	PER CENT
MICROWAVE FREQUENCY	2.45	GIGAHERTZ
MICROWAVE EFFICIENCY	80.	PER CENT
RANGE	35786.	KILOMETERS
PHASE SHIFT	22.50	DEGREES
[illegible] ANTENNA DIAMETER	8.00	KILOMETERS
TRANSMITTED POWER	7807.65	MEGAWATTS

RADIUS KILOMETERS	POWER DENSITY MILLIW/SQ.CM	EFFICIENCY PER CENT	RADIUS KILOMETERS	POWER DENSITY MILLIW/SQ.CM	EFFICIENCY PER CENT
.10	.12	.00	2.60	20.20	49.13
.20	1.68	.03	2.70	21.03	50.70
.30	6.71	.19	2.80	19.94	50.19
.40	15.14	.68	2.90	16.99	62.15
.50	23.77	1.63	3.00	13.88	65.50
.60	28.45	3.01	3.10	12.22	68.65
.70	27.22	4.54	3.20	11.98	71.64
.80	21.94	6.96	3.30	11.73	74.75
.90	16.11	7.12	3.40	10.36	77.00
1.00	12.31	8.11	3.50	8.11	79.87
1.10	10.90	9.08	3.60	6.26	81.60
1.20	10.86	10.12	3.70	5.56	83.34
1.30	11.25	11.30	3.80	5.06	85.04
1.40	11.72	12.62	3.90	5.28	86.70
1.50	12.10	14.08	4.00	4.20	88.08
1.60	12.16	15.65	4.10	3.09	89.09
1.70	12.14	17.31	4.20	2.43	89.91
1.80	12.98	19.19	4.30	2.41	90.75
1.90	15.59	21.67	4.40	2.58	91.69
2.00	19.67	24.72	4.50	2.20	92.43
2.10	23.04	28.61	4.60	1.67	93.01
2.20	24.07	32.87	4.70	1.10	93.43
2.30	22.53	37.05	4.80	1.04	93.81
2.40	20.31	40.97	4.90	1.18	94.29
2.50	19.47	44.89	5.00	1.16	94.76

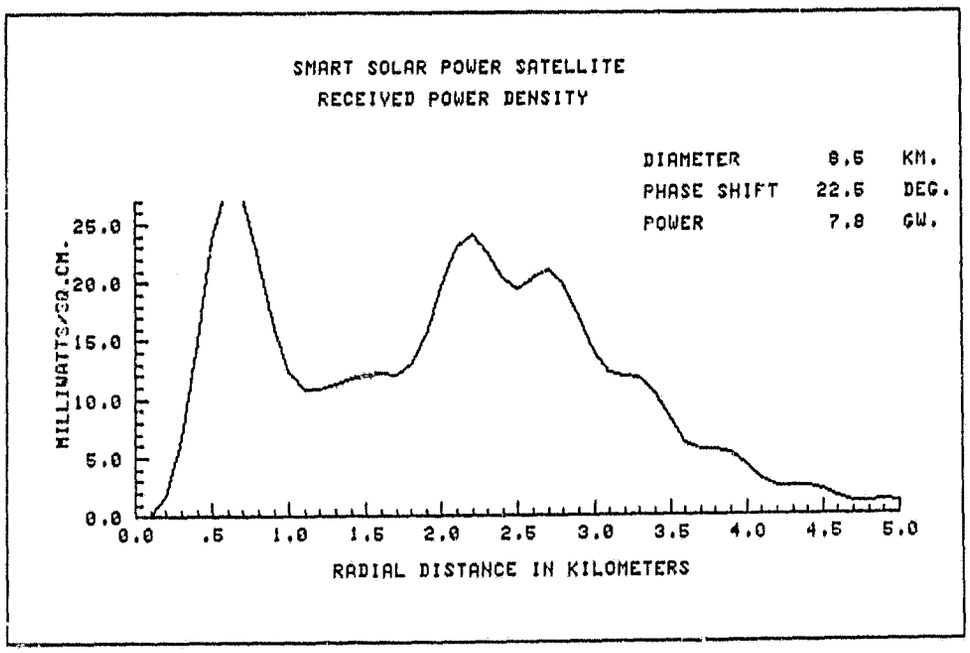

Figure II.7. SMART Solar Power Satellite - radiation calculation (phase shift = 22.5°).

SYSTEM PARAMETERS:

SOLAR CONSTANT	1350.	WATTS/SQ.METER
SOLAR CELL EFFICIENCY	13.	PER CENT
TRANSMISSION EFFICIENCY	90.	PER CENT
MICROWAVE FREQUENCY	2.45	GIGAHERTZ
MICROWAVE EFFICIENCY	80.	PER CENT
RANGE	35786.	KILOMETERS
PHASE SHIFT	-22.50	DEGREES
SMART ANTENNA DIAMETER	8.50	KILOMETERS
TRANSMITTED POWER	7807.65	MEGAWATTS

RADIUS KILOMETERS	POWER DENSITY MILLIW/SQ.CM	EFFICIENCY PER CENT	RADIUS KILOMETERS	POWER DENSITY MILLIW/SQ.CM	EFFICIENCY PER CENT
.10	6.99	.06	2.60	19.89	41.63
.20	6.42	.16	2.70	20.90	46.17
.30	8.03	.35	2.80	19.79	50.63
.40	12.40	.75	2.90	17.12	54.63
.50	17.45	1.45	3.00	14.75	58.19
.60	20.27	2.43	3.10	13.06	61.64
.70	19.57	3.64	3.20	13.97	65.24
.80	16.96	4.64	3.30	13.09	68.85
.90	14.90	5.71	3.40	11.68	72.10
1.00	14.58	6.88	3.50	9.48	74.77
1.10	15.20	8.23	3.60	7.71	77.00
1.20	15.18	9.69	3.70	7.15	79.13
1.30	13.74	11.13	3.80	7.11	81.30
1.40	11.38	12.41	3.90	6.87	83.37
1.50	9.09	13.51	4.00	6.30	85.07
1.60	7.60	14.49	4.10	3.95	86.38
1.70	7.35	15.49	4.20	3.27	87.48
1.80	8.68	16.70	4.30	3.25	88.61
1.90	11.57	18.02	4.40	3.25	89.76
2.00	15.14	20.96	4.50	2.79	90.77
2.10	17.80	23.90	4.60	2.02	91.52
2.20	18.51	27.24	4.70	1.49	92.08
2.30	17.73	30.52	4.80	1.43	92.63
2.40	17.16	33.84	4.90	1.55	93.24
2.50	18.05	37.47	5.00	1.46	93.83

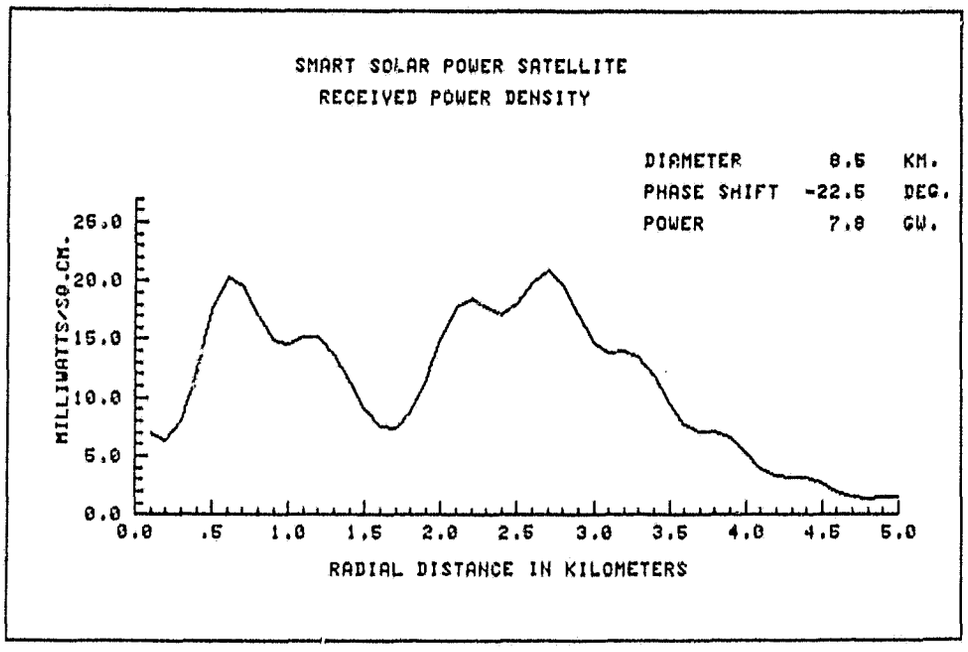

Figure II.8. SMART Solar Power Satellite - radiation calculation (phase shift = -22.5°).

III. DEVICE STUDIES

A. INTRODUCTION - PRELIMINARY ANALYSIS

The device-study portion of the program centered on designs for gallium arsenide field-effect transistors and emphasized the tradeoffs of

(a) power output versus efficiency;

(b) dc voltage versus efficiency.

The power-added efficiency of the power amplifier stages is obviously the dominant parameter in the solid-state SPS transmitter array, and the effect of efficiency optimization on the other operational characteristics of these amplifiers must therefore be carefully considered. A key factor in the development of high-efficiency amplifiers is the ability to study the current and voltage waveforms while the active device is operating under large-signal conditions. RCA recently developed a special measurement setup for the analysis of saturation phenomena in power MESFETs operating at 3 GHz. This measurement system, consisting of a computer-controlled sampling oscilloscope and associated hardware, is described in Ref. 3. A copy of this paper is attached as Appendix A.

Some of the conclusions reached from the previous study with this equipment are very pertinent to the amplifiers used in the solid-state SPS transmitter. Specifically, we found that when a power MESFET is biased and tuned for maximum output power and efficiency, the peak voltage between gate and drain exceeds the breakdown of the Schottky barrier. We noticed that power saturation was caused by breakdown and forward conduction of the Schottky barrier and not by voltage clipping or current saturation on the drain. In the design of high-efficiency amplifiers particular attention will have to be paid to limiting the peak voltage across the Schottky barrier. The waveform measurement system will be important in these design efforts.

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3. F. Sechi, H. Huang, and B. Perlman, "Waveforms and Saturation in GaAs Power MESFETs," Proc. 8th European Microwave Conf., Paris, France, Sept. 1978.

This approach will acquire even greater importance when the devices are operated in a Class E mode [4,5]. In principle, this mode of operation, which relies on fast switching of the device from an "on" to an "off" state, results in a very high efficiency, but is difficult to implement because of the device limitations.

The desirability of using *higher-voltage FETs* is related to the problem of voltage distribution and is therefore of particular concern when one attempts to replace the high-power klystrons (or other thermionic devices) with solid-state amplifier clusters in the Reference System. However, higher-power and higher-voltage device designs entail penalties in efficiency which must be weighed carefully.

A typical device design for 20-V operation at 2.45 GHz involves a charge density of 4×10^{16} cm^{-3}, a thickness of T = 0.6 μm, and a device gate length of ℓ_3 = 2.5 μm. This is predicted to yield unit cells providing 1.5 W of output power, a gain of G = 12 dB, and an efficiency of about 60%. If eight such unit cells were to be combined, the combination loss would be 0.6 dB, yielding a power output of 10.45 W at an efficiency of 52% -- clearly too low for SPS purposes. In a more general way, there is a basic *power output* vs efficiency tradeoff in power FETs. The theoretical relationship between the wave shape (and conduction angle) and the efficiency on one hand, and the conduction angle θ and the power degradation factor on the other, indicates that the best compromise between power and efficiency is for conduction angles between 30° and 45°. The maximum theoretical efficiency is 90%, but this is the limiting case for zero conduction angle and no power output. At the other extreme, for maximum power output obtainable with a given device (θ = 90°), the theoretical efficiency is 64%. The best compromise between power and efficiency is for conduction angles between θ = 30° and θ = 45°. For θ = 30°, only *one-half* the maximum power can be obtained at a theoretical efficiency

4. N. O. Sokal and A. D. Sokal, "Class E, a New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers," IEEE J. Solid-State Circuits SC-10(3), 168-176 (June 1975).
5. F. Raab, "Effects of Circuit Variations on the Class E Tuned Power Amplifier," IEEE J. Solid-State Circuits SC-13(2), 239-247 (April 1978).

of 85.5%. For $\theta = 45°$, 0.707 P_{max} is achievable at an efficiency of 81%. High-efficiency amplifiers will have to fall within the above limits.

The first design considered in the study was a Schottky-barrier gate FET (MESFET), a device now widely used for low-noise and medium-power microwave amplifiers, including those used in spaceborne systems.

In Fig. III.1 (, depicted a sketch schematically representing a Schottky-gate FET. In a MESFET, the Schottky-barrier gate contact is essentially in the same plane as the source and the drain contacts. The gate metallization is defined either by careful alignment fixturing or by a self-aligned fabrication approach. The detailed process steps for the fabrication of self-aligned gate FETs are described in Appendix B. The alternative process for the definition of a FET gate is similar to the self-aligned process except that an additional photolithographic step is required to precisely align the gate between the source and the drain.

In Appendix B, we have shown that it is possible to package the MESFET in flip-chip form, so that the heat generated in the FET channel can be conducted through plated-up metal rather than through the GaAs substrate. In addition, the parasitic source inductance of a flip-chip-mounted FET can be kept at a minimum.

In the more detailed analyses of two different types of FETs we have concentrated on maximizing the device efficiency, with only secondary emphasis on extracting the maximum power from a specific design. Since, as became apparent from the system and module portions of the study, the recommended concept of the solid-state SPS transmitter appeared to be clearly favoring a SMART-type approach, the lower-voltage versions of the designs did not represent a limitation from the ultimate system point of view.

B. FET DESIGNS

1. Analysis of High-Efficiency MESFET

The theory of operation and the design model for a GaAs MESFET is fully described in Appendix B. When applied to a high-efficiency design for 2.45-GHz operation, these principles lead to a sample design having the following device parameters:

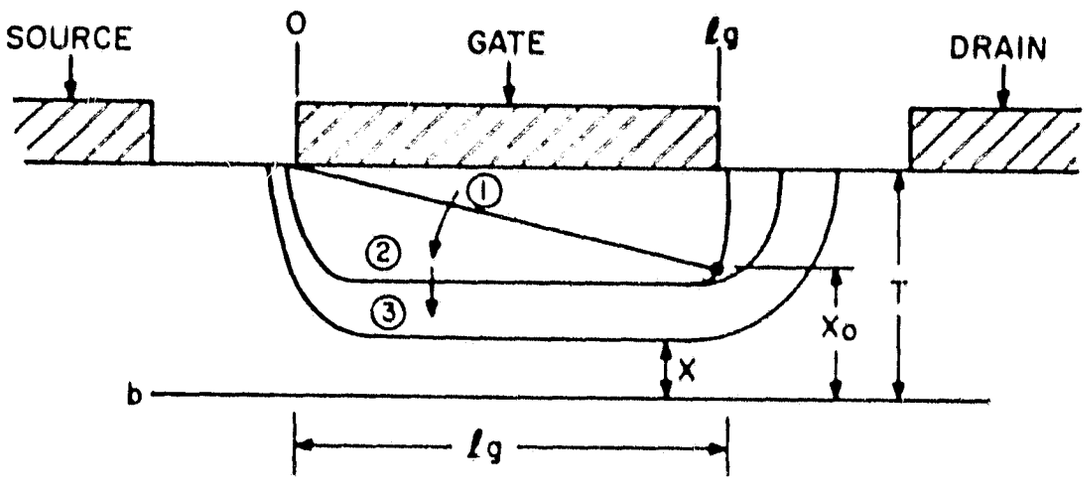

Figure III.1. Cross section of gate with various stages of carrier depletion of the channel.

Carrier Concentration:	$n = 6 \times 10^{16}$	cm^{-3}
n-Layer Thickness	$T = 5 \times 10^{-5}$	cm
Gate Length	$\ell_g = 1.5$	μm
Total Gate Width	$W_t = 7$	mm

The maximum voltage swing is $V_{max} = 18$ V and $\Gamma = 0.81$. Therefore, the maximum output power for a MESFET with 7-mm gate width is 5.6 W. Under Class E operating conditions with a conduction angle of 45°, the maximum efficiency is 81% with an output power of 3.9 W.

2. JFET Design

Most GaAs transistors are designed for operation at the higher microwave frequencies (4 GHz and above), for which the MESFET configuration is more ap-

propriate. At the SPS frequency of 2.45 GHz, however, the junction transistor (JFET) may have applicability, and we have therefore carried out an analysis of a JFET design which is presented in this section.

A sketch of a JFET is shown in Fig. III.2.

The output power of a FET can be expressed as (see Appendix B)

$$P_{out} = \frac{1}{8} V_{max} V_m \Gamma \qquad (5)$$

where V_{max} is the maximum voltage (dc + rf) that can be applied to the device, n is the carrier concentration, e the electronic charge, W the gate width, T the thickness of the channel, $V_m = 10^7$ cm/s is the saturation velocity, and $\Gamma \approx 0.8$ is a degradation factor due to the presence of a finite output conductance. An optimal set of device parameters for 2.45-GHz operation is:

Carrier Concentration:	$n = 3 \times 10^{16}$	cm^{-3}
Channel Thickness	: $T = 6 \times 10^{-5}$	cm
Gate Length	: $\ell_g = 1.5$	μm
n-Layer Thickness	: $\ell_n = 0.9$	μm
Total Gate Width	: $W_t = 7.0$	mm

The pn junction voltage for this FET is calculated to be 35 V. The pinchoff voltage V_p for this FET is 4 V, and the saturation voltage V_s is about 2 V. Therefore, the maximum allowable peak-to-peak rf swing V_{max} is given by

$$V_{max} = V_B - V_p - V_s = 29 \text{ V}$$

The maximum output power is thus 6 W. When this device is operated under Class E conditions with a conduction angle of 45°, the theoretical maximum efficiency is calculated to be 81% with an output power of 4 W.

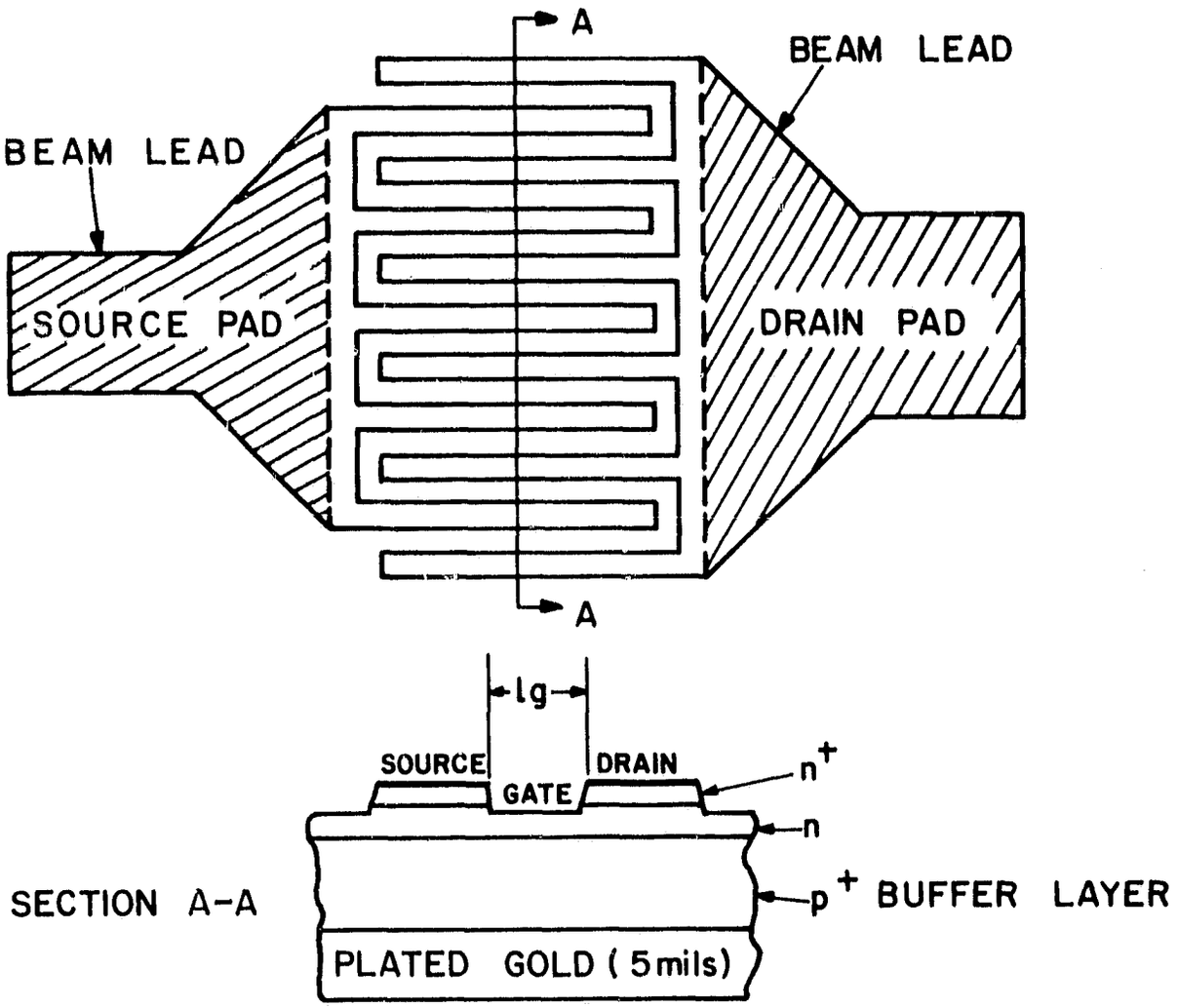

Figure III.2. Single-cell common gate FET. GaAs under the shaded area is removed for the reduction of stray capacitances.

3. Thermal Analysis - JFET/MESFET Comparison

In order to reduce the source-gate and drain-gate capacitance of a JFET, the source and the drain interdigital finger lengths are kept as small as possible. A length of the order of 5-10 μm is preferred for achieving both small capacitances and small resistances in the interdigitated fingers. Because of the rather small finger length, the JFET has to be mounted substrate-side down. Thermal flux generated at the FET channel has to flow through the GaAs substrate, which has high thermal resistivity. This is in contrast to the situation with the flip-chip-mounted MESFET, as previously explained.

We have carried out theoretical calculations of FET thermal resistance for both the substrate-side down and the flip-chip cases. This is included in Appendix C. The thermal resistance of a FET-mounted substrate side down depends heavily on the substrate thickness, as expected. Under normal conditions, a substrate thickness of 100 μm can be achieved. It is possible to reduce the substrate thickness to 25 μm by a slightly more complicated fabrication procedure. We will calculate the operating temperature rise of a JFET with a 25-μm-thick substrate as compared to a MESFET. We will also calculate the degradation in performance of a JFET due to its operating temperature being higher than that of a MESFET. From Fig. C-2 of Appendix C, we find that the thermal resistance of a JFET with 7-mm gate width and 10-μm source and drain widths is 14°C/W. A flip-chip-packaged MESFET with the same gate width would have a thermal resistance of 7.5°C/W. When an output power of 4 W, a power-added efficiency of 65%, and a gain of 10 dB are assumed, the dc input power is 5.54 W. The power dissipated is 1.94 W. The temperature rise is therefore 27°C for a JFET and 14.5°C for a MESFET. This difference in temperature rise is not large enough to cause any appreciable change in drift mobility and rf performance.

The source inductance of a JFET can be kept small by use of a gold ribbon bond from the source pad to the rf matching network. This source inductance is comparable to the ribbon inductance of a flip-chip MESFET between the gate pad and the rf matching network. Therefore, we do not expect a substantial degradation in rf performance resulting from the source ribbon inductance.

The above calculations indicate that the performance of a JFET is roughly comparable to that of a MESFET for the SPS application. Experimental effort to verify the theoretical calculation as well as an accurate theoretical model would be required to make a more definite recommendation as to the basic FET configuration to be used in the SPS transmitter.

C. AMPLIFIER MEASUREMENTS

Although the assembly of an experimental amplifier was not contemplated in the original Work Statement, measurements on such a unit were judged important as the study progressed and -- with the concurrence of the Technical Monitor -- a power amplifier stage using a commercial FET (FLC 30) was assembled and tested as part of the program. The microwave circuit, built with microstrip lines on Al_2O_3 substrates, was computer-designed and experimentally optimized for operation at maximum power-added efficiency. We measured a maximum power-added efficiency of 58.5% with an output power of 3.05 W and an associated gain of 6.8 dB. The output power and power-added efficiency as functions of rf input drive are shown in Fig. III.3, together with some of the operating characteristics. The measurement results are tabulated in Table III.1.

The device operated in Class AB with the bias optimized for maximum efficiency. Since the gain of the device is not very high, the effect of the input power on the power-added efficiency is rather high. In fact, at the maximum efficiency point, the drain efficiency reaches a value of 75%; this indicates that a major improvement in power-added efficiency can still be achieved by increasing the gain.

We also noticed that, for high-efficiency operation, the tuning of the circuits becomes unusually critical, which is probably due to variations in the shapes of the voltage and current waveforms at the gate and the drain of the FET. We suspect that the third harmonic, at 7.35 GHz, has a great effect on the output power and efficiency at 2.45 GHz. The optimization of the device operating parameters and of the device-circuit interaction becomes exceedingly difficult to handle with simple experimental techniques. In order to attain truly optimum performance, we believe it necessary to carry out a careful analysis and control of the waveforms in the active device.

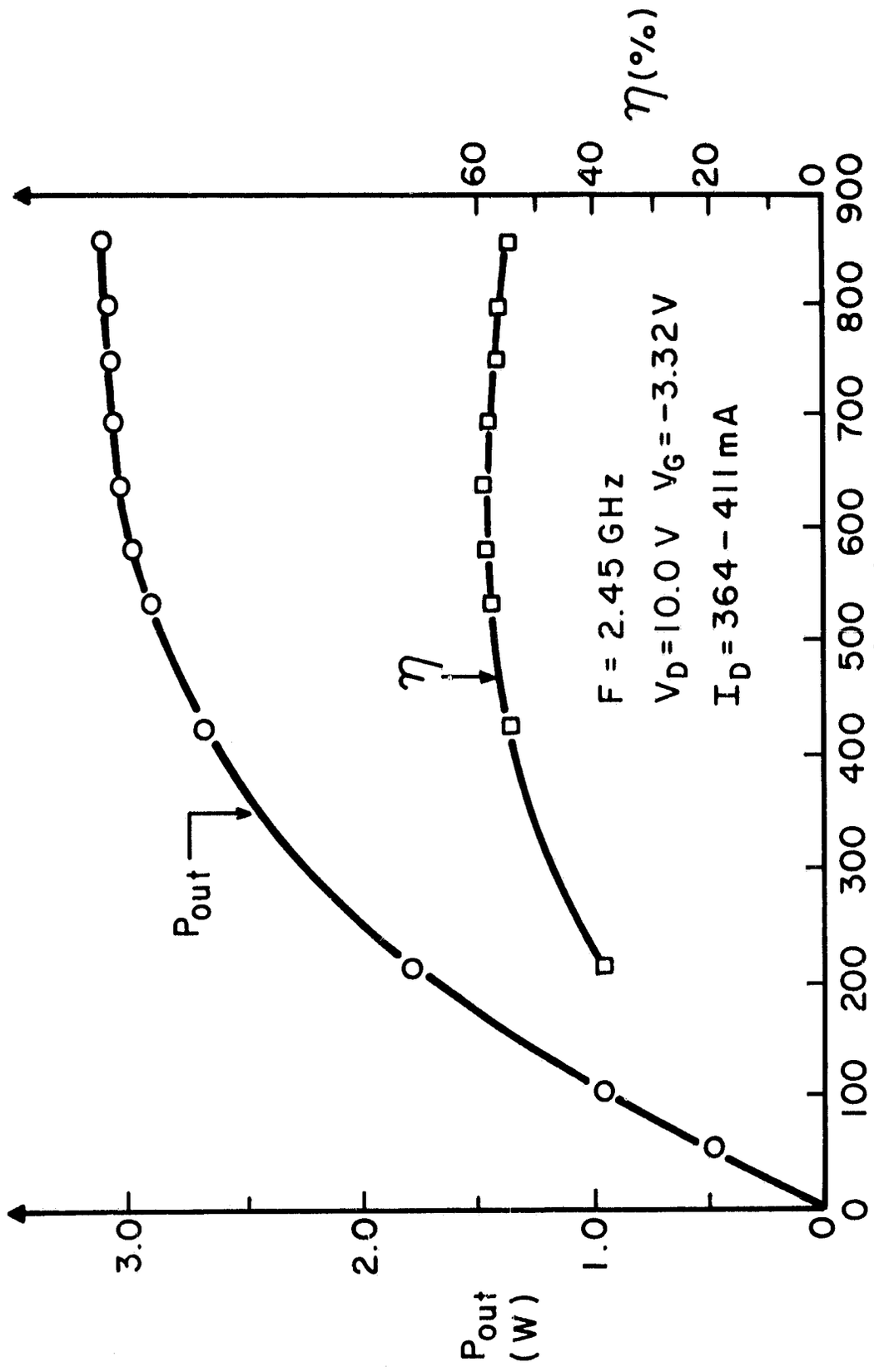

Figure III.3. Output power and power-added efficiency vs input power.

TABLE III.1. TEST ON EXPERIMENTAL POWER STAGE - FLC 30, FET #441

V_d (V)	V_G (V)	I_d (mA)	P_{in} (mW)	P_{out} (mW)	G (dB)	η (%)
10.02	-3.37	364	54.4	483	9.5	
		385	106.8	978	9.6	
		410	213.7	1789	9.2	
		411	427	2680	8.0	
		411	534	2916	7.4	57.9
		411	587	3001	7.1	58.7
		409	641	3049	6.8	58.8*
		408	694	3078	6.1	58.4
		408	748	3096	6.2	57.4
		409	801	3115	5.9	56.6
		411	855	3134	5.6	55.4

*Best efficiency.

The above measurements were performed with the FET carrier and matching-circuit elements not permanently affixed. For the delivery to NASA, the amplifier (using the same transistor) was reworked, the unit was reoptimized, and the circuit elements were soldered. A photograph of the amplifier is shown in Fig. III.4. The operating data of the unit are presented in Table III.2. It will be seen that the performance varies somewhat from the initial data. (The maximum efficiency measured on the amplifier was 58% at an output power of 3.065 W, compared to the previous measurement of 58.8% at 3.049 W.)

Note: In making measurements on this amplifier, it should be placed on a heat sink maintained at room temperature or below. The recommended values for V_G and V_d are -4.01 V and +10.14 V, respectively. In turning the amplifier on, $-V_G$ should be turned on first, then $+V_d$. In turning the unit off, $+V_d$ should be turned off first, then $-V_G$.

TABLE III.2. TEST ON HIGH-EFFICIENCY 2.45-GHz POWER AMPLIFIER (DELIVERABLE VERSION)

V_d (V)	V_G (V)	I_d (mA)	P_{in} (mW)	P_{out} (mW)	G (dB)	η (%)
10.14	-4.01	259	77.1	505.4	8.2	16.4
		274	103.5	709	8.3	21.8
		286	127.1	882.2	8.4	26.0
		300	152.8	1054.2	8.4	29.6
		326	199.2	1401.7	8.5	36.4
		348	250.6	1755	8.4	42.6
		364	315.6	2070.9	8.2	47.7
		374	377.7	2304.9	7.6	50.8
		386	474.1	2609.1	7.4	54.6
		391	519.1	2737.8	7.2	56
		396	582.6	2889.9	6.9	57.5
		399	642.6	2983.5	6.7	57.9
		399	681.9	3030.3	6.5	58.0
		400	714	3065.4	6.3	58.0

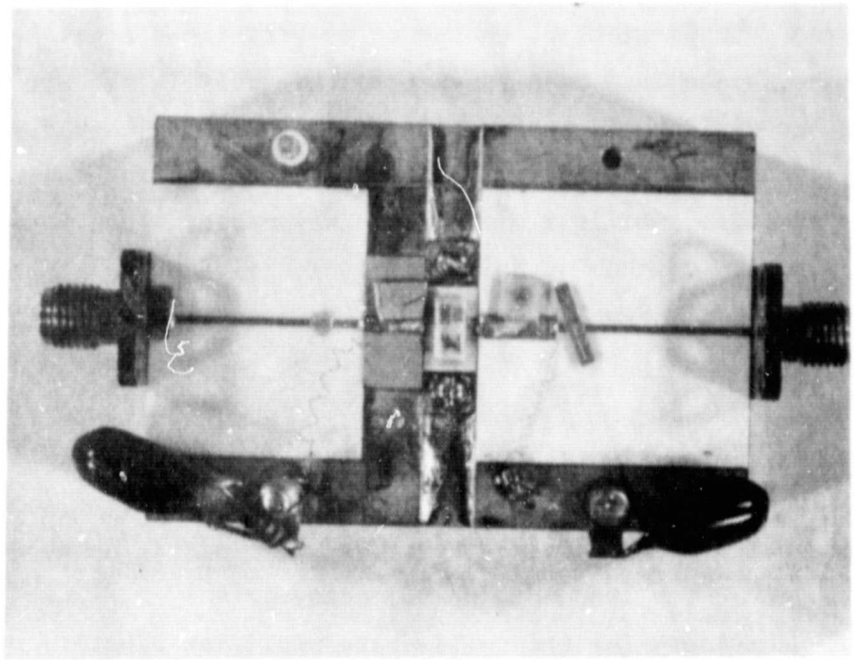

Figure III.4. Photograph of high-efficiency power amplifier stage (deliverable version).

IV. MODULE STUDIES

A. INTRODUCTORY ANALYSIS

For purposes of this study, we define a *microwave module* as the transmitter elements that convert solar energy into microwave energy, amplify the microwave power, and direct the microwave power to an element of the transmitting antenna array at the correct phase to generate the microwave beam. (The antenna elements themselves also form part of the "module.")

An approximate allocation of system costs per watt of output power may be as follows:

Structure and Solar Cells:	15%	($0.23/W)
Construction in Space:	10%	($0.15/W)
Launch:	45%	($0.67/W)
Rectenna:	20%	($0.30/W)
Microwave Module:	10%	($0.15/W)
Total	100%	($1.50/W)

Module efficiency has a pronounced effect on overall system design, and design tradeoffs involving optimization for efficiency must therefore be carefully considered. In particular, the power-vs-efficiency consideration is of great importance, since this is a fundamental tradeoff in the FET devices. The combining and dividing losses involved in paralleling many devices strongly affect module efficiency. The economics of feeding a number of antennas from a single amplifier are also questionable, since the circuit losses as well as device-combination losses quickly decrease overall efficiency to unacceptable levels. Finally, studies of dc power distribution systems have led us to concur with the findings of the Rockwell Third Quarterly Review (12/16/78):

(1) The power conditioning system required for a solid-state design in which the klystrons are replaced by clusters of solid-state amplifiers incurs a severe weight penalty even if the very optimistic dc-to-dc converter performance projected for 1988 were to be achieved.

(2) Power combiners for the solid-state amplifier clusters will impose a severe penalty in efficiency.

We are thus led to the conclusion that *a system design in which a multiplicity of low-power modules derive their energy directly from the elements of the solar-cell array* is the preferred approach to the solid-state SPS transmitter, since in such a system the efficiency penalties of the microwave modules as well as both the efficiency and weight penalties of the dc distribution system are not incurred.

Accepting this approach, it becomes of interest to determine the module power limits based on utilization of available solar power.

An assumed maximum antenna spacing is 4λ, taking into consideration that increasing antenna spacing leads to poorer steerability, higher sidelobes, and more complex individual antennas.

For $\lambda = 12$ cm and a spacing of 4λ, the total area/modules is 2304 cm^2. Total dc power available from solar panels is $2304 \times 0.015 = 34.6$ W. If an amplifier efficiency of 80% is assumed, power output is 27.6 W (higher power devices have lower efficiency).

Thus, an upper limit of power is about 30 W/module, if power combining in the amplifier and power dividing into several antennas are excluded.

A similar calculation for the lower limit of power/module when a $\lambda/2$ antenna spacing is used (providing good beam steering and low sidelobes) yields an area/module of 36 cm^2 and 540 mW of available dc power. With an 85% device efficiency the maximum output power is 460 mW. Here there are not thermal or impedance problems, and the device efficiency is close to theoretical -- but the number of elements is prohibitively high.

A possible compromise may be the use of two 1.5-W devices working in push-pull, Class E. An efficiency of 85% can be expected, and the impedance and voltage of the devices can be designed to provide a direct match to the antenna.

B. MODULE DESIGNS

The following two designs, based on a transmitting antenna concept utilizing 3-W microwave modules with dipoles spaced on a $1.3\ \lambda \times 1.3\ \lambda$ grid, were investigated further. In this arrangement, 16-module clusters providing about 50 W of transmitter power would be employed, all controlled from a single receiver module which would include the phase-control circuitry for the 50-W cluster. Two separate module/dipole configurations have been

considered, the common idea being the placement of the amplifiers in direct contact with the antenna dipoles, the metallization of the dipoles thus providing effective heat-dissipation areas.

1. High-Q Design

In this arrangement the antenna elements are printed on a 3-mil Kapton sheet spaced $\lambda/4$ away from the (metallized) back surface of the solar-cell blanket. The amplifiers use two 1.5-W devices in push-pull. Each amplifier uses lumped-element circuits and "bump"-mounted GaAs FETs, all on a 0.5-cm x 1-cm sapphire substrate. The modules are fed by balanced lines from the receiver and are supplied with dc power via feed lines extending across the space from the solar blanket to the antenna sheet (see Fig. IV.1).

2. Patch-Resonator Design

This concept envisages a 20-mil-thick plastic grid between the solar blanket and the antenna elements. Here the circuit efficiency is lower, and single 3-W chips are employed in the two-stage amplifier (see Fig. IV.2).

The two arrangements represent essentially a tradeoff between efficiency and mechanical complexity. The high-Q design requires much easier impedance-transformation designs between the amplifier and the antenna, while the patch resonator antenna is simpler, but less efficient. Both approaches represent designs with a weight of *less than 1 g/W,* compared to the Reference System figure of 1.5 g/W.

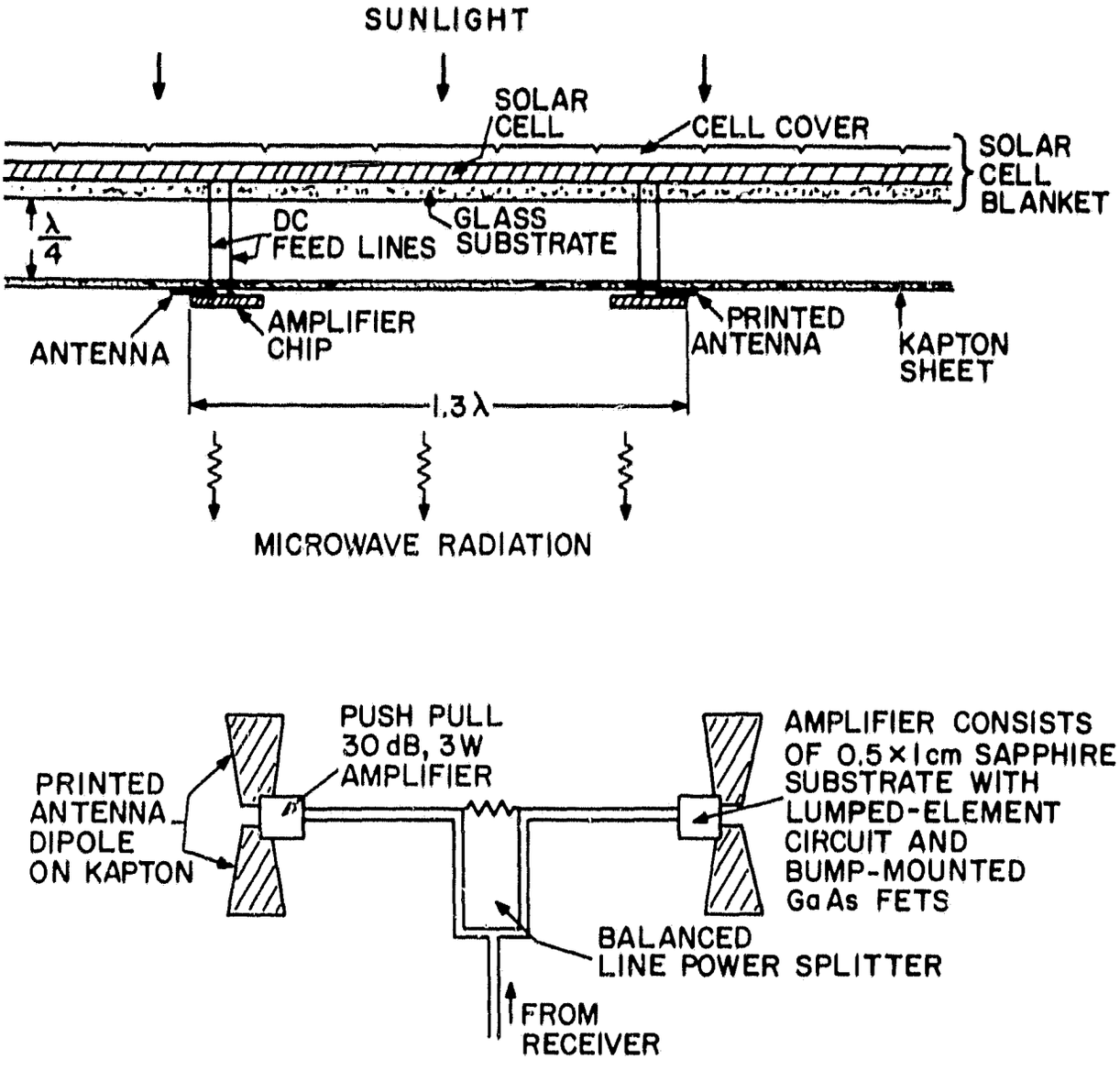

Figure IV.1. High-Q design.

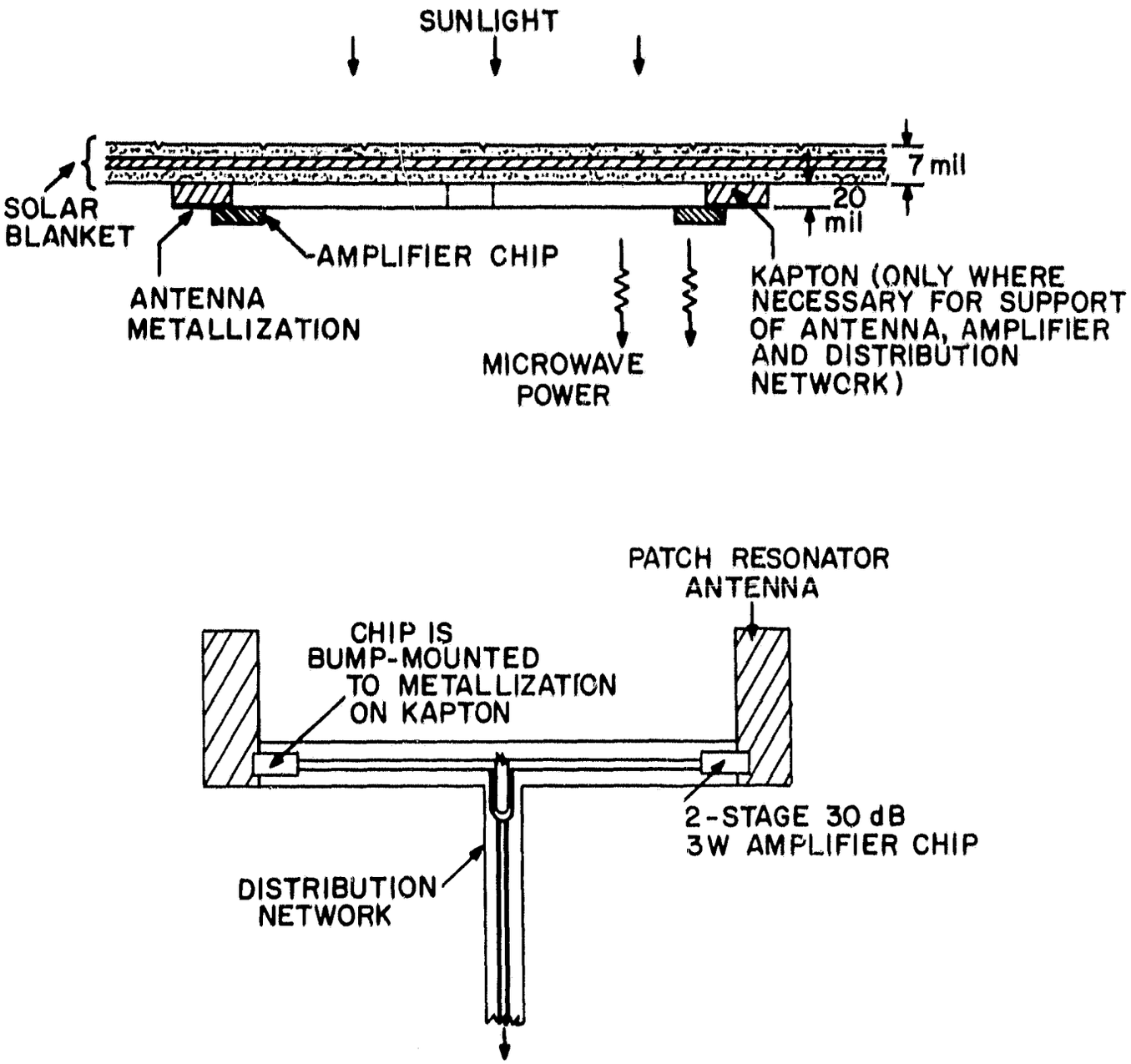

Figure IV.2. Patch-resonator design.

V. CONCLUSIONS AND RECOMMENDATIONS

A. SYSTEM CONSIDERATIONS

We conclude that the simple replacement of the SPS transmitting antenna using klystrons by a solid-state transmitter in the Reference System design is not advisable for the following reasons:

1. The Reference System design leads to smaller transmitting antennas as the system power increases, requiring a high power density. To avoid the high temperatures which follow from high power density, an extensive cooling system is required; this entails a considerable mass.

2. If the system power is reduced so that the power density becomes suitable for solid-state devices, the power distribution and conditioning system must be increased in mass to accommodate the inherently low voltage, high current solid-state devices.

3. Reference System designs for 2-GW systems using solid-state devices will require moderately high module powers which will have to be realized by combining the microwave outputs of a number of devices. This power combining will tend to reduce the overall efficiency of the microwave transmitter.

We estimate that a 2-GW solid-state system using the Reference System design will have a specific power figure of merit which is 30% below that of the klystron Reference System. Specifically, the system power to satellite mass is estimated at 122 W/kg for the Reference System, and 86 W/kg for the solid-state replacement.

By the use of the SMART (Solar Microwave Array Technology) concept, a more advantageous system can be designed. When the solid-state devices are directly coupled to solar-cell modules, the temperature, power distribution, and combiner limitations are eliminated. By use of the properties of the Fresnel zone or near field, large SPS systems can be designed which maintain a low power density and low increase in area as the system power increases. We find that the specific power figure of merit for the SMART System is 10% above that of the Reference System. Specifically, the SMART System yields 138 W/kg compared to the Reference System figure of 122 W/kg.

The major disadvantage of the SMART System is the requirement for a mirror system to provide constant solar illumination of the array as the satellite traverses its geostationary orbit. A number of RCA proprietary proposals are under consideration for the simplification or elimination of the mirrors. The mirror area can also be increased to provide a higher solar concentration ratio on the array.

We make the following recommendations for continuing system studies:

1. The near-field antenna patterns should be calculated in greater detail. In addition, the antenna-phasing requirement should be studied to determine the permissible tolerances in phase deviation and error.

2. The near-field study should be extended to the consideration of uniform illumination on sidelobes and grating lobes.

3. A detailed study should be made of the proposals to simplify or eliminate the mirror system required for the SMART System.

B. MODULES/DEVICES

Optimization of microwave module efficiency is undoubtedly the next major task of the solid-state SPS transmitter concept development. The FET amplifiers will probably operate in Class E, which relies on fast switching of the devices. Device limitations in this mode of operation are largely unknown and must be investigated.

Important instrumentation for large-signal analysis of power FET amplifiers has been developed by RCA (see Appendix A). We recommend that this tool be used in determining the complex waveforms existing in a FET amplifier operating in Class E, and that this information be used to optimize *both device and amplifier circuit designs for high efficiency and reliability.*

REFERENCES

1. G. Goubau, "Microwave Power Transmission from an Orbiting Solar Power Station," J. Microwave Power 5, 4 (1970).

2. J. F. Ramsay, "Tubular Beams from Radiating Apertures," Vol. 3 of Adv. Microwaves (Academic Press Inc., New York, 1968).

3. F. Sechi, H. Huang, and B. Perlman, "Waveforms and Saturation in GaAs Power MESFETs," Proc. 8th European Microwave Conf., Paris, France, Sept. 1978.

4. N. O. Sokal and A. D. Sokal, "Class E, a New Class of High-Efficiency Tuned Single-Ended Switching Power Amplifiers," IEEE J. Solid-State Circuits SC-10(3), 168-176 (June 1975).

5. F. Raab, "Effects of Circuit Variations on the Class E Tuned Power Amplifier," IEEE J. Solid-State Circuits SC-13(2), 239-247 (April 1978).

APPENDIX A

WAVEFORMS AND SATURATION IN GaAs POWER MESFETs

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ABSTRACT

Measurements of voltage and current waveforms in power MESFETs have shown that voltage breakdown of the Schottky barrier is responsible for power saturation and consequent nonlinearity of MESFET amplifiers. Also, high peak drain-gate voltages affect device reliability and noise in FET oscillators.

INTRODUCTION

The direct measurement of voltage and current waveforms in power MESFETs (Metal Schottky barrier FETs) operating at microwave frequency is of considerable interest since distortions of these waveforms affect the linearity as well as the output power of the devices. Also, phenomena occurring in a device operating under large signal conditions have implications in such diverse areas as FET oscillator noise or FET reliability. Moreover, information gained from these experiments is considered important for the design of FETs featuring improved output power, linearity, noise and reliability.

VOLTAGE AND CURRENT WAVEFORMS

The waveform measurements were carried out with the aid of a computer-controlled sampling oscilloscope and a Fast Fourier Transform algorithm [1]. Figure 1 is the block diagram of the measurement setup. The vertical outputs from the two channels of the sampling oscilloscope are digitized by a scanning DVM and are fed into the computer. These data are stored and processed with a Fast Fourier Transform algorithm. The current waveforms are then computed from the measured response of the probing circuits and from the impedance of the circuits surrounding the FET. This technique is very accurate and allows easy computation of waveforms at points inaccessible to the probe. In effect, all the waveforms shown here are those computed at the FET pellet.

Figure 2 shows the drain and gate waveforms in a power MESFET operating at 3 GHz. The bias is +6.0 V and 330 mA for the drain and -2 V for the gate. Notice that at the drain the current is almost in phase with the voltage. At the gate, instead, the current leads the voltage by almost 90°. The device is already partially saturated with a gain compression is 0.5 dB. Yet, surprisingly, the drain waveforms don't show any appreciable sign of voltage clipping or current limiting. The gate voltage waveform, instead, is already heavily distorted. When the gate is most negative (-4.4 V) the drain is most positive (+ 11.5 V) which results in a gate to drain voltage

of 4.4 + 11.5 ≯ 16 V. This high peak voltage causes a breakdown of the Schottky barrier with consequent flow of DC current in the gate circuit. Figure 3 shows the waveforms at an increased input RF power corresponding to a gain saturation of 1.0 dB. At this point the device is delivering 750 mW of output power. In spite of the saturation of the output power, the drain waveforms are still sinusoidal. A further increase of the input RF power results in the waveforms shown in Fig. 4. The device now is heavily saturated, yet the drain waveforms are still sinusoidal. The gate voltage waveform, instead, is highly distorted and the Schottky barrier is alternately driven from conduction (positive v_g) to breakdown. At a gate bias of -3.0 V, Fig. 5, some distortion appears in the drain waveforms. The gate to drain voltage reaches 18.5 V, which drives the Schottky barrier heavily into breakdown.

When the drain voltage is raised to 8.0 V, Fig. 6, the drain waveforms regain a sinusoidal shape while the gate voltage waveform remains highly distorted: the gate to drain voltage reaches approximately 21 V which drives the Schottky barrier into heavy breakdown. This certainly reduces the life of the device. These waveforms clearly show that the saturation of these MESFETs is caused by the reverse voltage breakdown and forward conduction of the gate Schottky barrier. In other words, saturation and output power are determined by the characteristics of the control element (gate) and not by drain voltage clipping or drain current saturation.

Further evidence of this phenomenon is shown in Fig. 7 where the output power and the DC gate current are plotted as functions of the input power. Appreciable power saturation occurs when the breakdown current is 100 μA. An increase of RF drive increases I_g up to the point where the Schottky barrier starts to be driven into conduction. Since the conduction current is opposite to the breakdown current, an increase of the input power, at this point, results in a decrease of the total gate current. With a large enough drive, the gate current changes direction and becomes negative.

VOLTAGE BREAKDOWN AND OSCILLATOR NOISE

The voltage breakdown of the Schottky barrier could lead to a significant increase of the noise in FETs operating under large signal conditions. This was proven by forcing a FET into oscillation -- which develops large signals -- and by analyzing the output spectrum under different gate current and bias conditions. The setup used is shown in Fig. 8. The device, whose waveforms are shown in Figs. 2-6, is mounted on a fixture that includes input and output RF tuning. A fraction of the output power is fed to the input through a high-pass resonator and a variable attenuator which allows feedback control. A fraction of the output power is also sent to a diode detector through a frequency discriminator and a 3-dB coupler. The power in the detector, equal to P_d, was kept constant throughout the experiments at a value of 3 mW. The detected signal is analyzed by a selective voltmeter (Wave Analyzer). Power meters measure the FET input and output RF powers. The frequency discriminator was removed during AM measurements. Since noise in the oscillator is strongly affected by the circuit surrounding the device [2,3] care was taken to present to the device constant impedances under all conditions. The noise is also a function of the degree of saturation of the device, as this affects the low-frequency noise upconversion. In order to achieve an approximately constant degree of upconversion, under different bias conditions, the feedback was adjusted to maximize the power generated by the device (P_{out}-P_{in}).

Figure 9 shows plots of the AM noise-to-signal ratio (NSR) as a function of the modulation frequency (F_m). The two curves are the performances at two different biasing conditions. At 1 kHz away from the carrier, for example, the noise levels for the two conditions differ by more than 7 dB. Similar performances were measured at different biasing voltages. Most interesting was to list the AM noise, at F_m = 1 kHz for instance, as a function of the peak breakdown current (I_{gb}), as shown in Table I. Clearly, with the exception of the last test, there is an excellent correlation between high AM noise and high breakdown currents. The last test, instead, shows an unusually high forward conduction current (I_{gc}). Since forward conduction current develops a negative resistance in the gate bias circuit, probably noise amplification is responsible for the increased oscillator noise.

Good correlation also exists between FM noise and gate breakdown currents, as shown in Table I. The highest FM noise corresponds to the highest breakdown current. Also highest and lowest FM noise were measured at those conditions that resulted in highest and lowest AM noise, respectively. Curves of FM noise as a function of the modulation frequency are shown in Fig. 11. It is interesting to note that the AM and FM noise performance at the lowest drain and gate voltages compare quite favorably with those of the low noise klystrons.

CONCLUSIONS

In conclusion, we showed that major factors limiting the power output of a MESFET and causing saturation of the device are the reverse voltage breakdown and the forward conduction of the Schottky barrier. In other words, the output power is limited by the characteristics of the control element (gate) and not by current saturation or voltage clipping in the drain circuit. Also, the high voltages between gate and drain result in a reduction of device reliability and in an increase of the device noise. This increase of internal noise, due to voltage breakdown of the Schottky barrier, has been shown to affect the noise of FET oscillators. Still, proper biasing and proper RF design results in noise performance that compare favorably with those of klystrons.

REFERENCES

1. F. N. Sechi, H. C. Huang, B. S. Perlman, "Voltage and Current Waveforms in Power MESFETs at Microwave Frequencies," Digest of 1978 International Solid-State Circuits Conference, San Francisco, pp. 168-169.

2. R. Muller, "Noise in Microwave Oscillators," Proceedings of 4th Biennial Cornell Conference, 1973, Ithaca, N.Y., pp. 21-32.

3. H. Thaler, G. Ulrich, G. Weidmann, "Noise in Impatt Diode Amplifiers and Oscillators," IEEE Transactions MTT, Vol. 19, No. 8, August 1971, pp. 692-705.

TABLE I

V_d (V)	V_g (V)	I_{gb} (μA)	I_{gc} (mA)	NSR @ 1 kHz (dB)	ΔF_{rms} @1 kHz (Hz)
+6.0	-3.0	+6500	0	-114.5	23.6
+8.0	-2.0	+980	-1.15	-117.5	11.9
+6.0	-2.0	+194	-2.28	-119.5	18.3
+5.0	-2.0	+ 87	-3.62	-122.0	10.6
+6.0	-1.0	+4.8	-19.3	-118.5	12.2

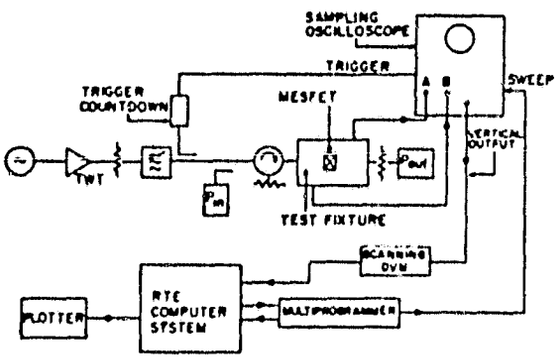

Fig. 1 Waveforms Measurement Setup.

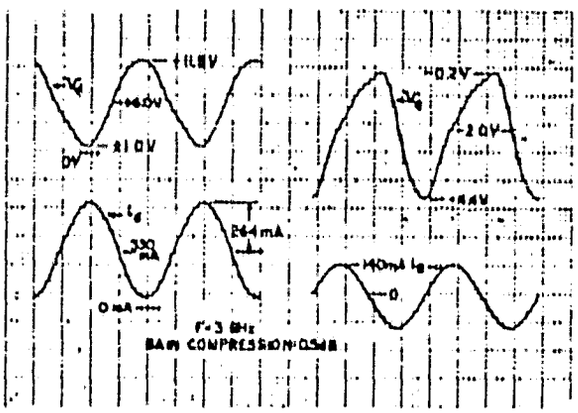

Fig. 2 Waveforms at V_d=+6.0 V, I_d= 330 mA, V_g=-2.0 V and 0.5 dB gain compression.

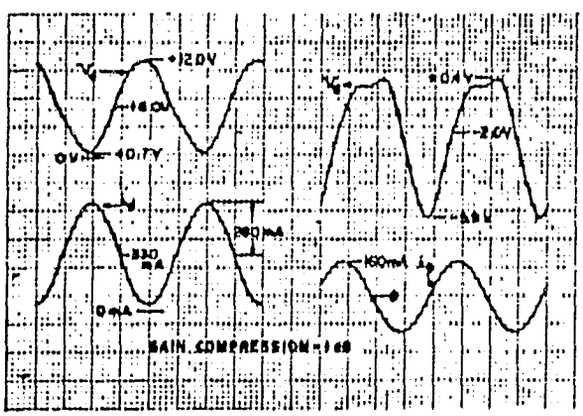

Fig. 3 Waveforms at V_d=+6.0 V, I_d= 330 mA, V_g=-2.0 V and 1 dB gain compression.

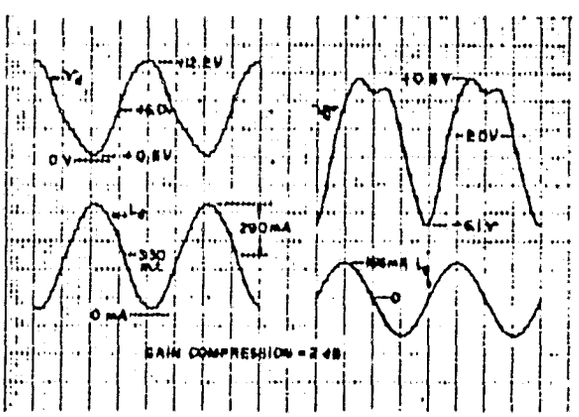

Fig. 4 Waveforms at V_d=+6.0 V, I_d= 330 mA, V_g=-2.0 V and 2 dB gain compression.

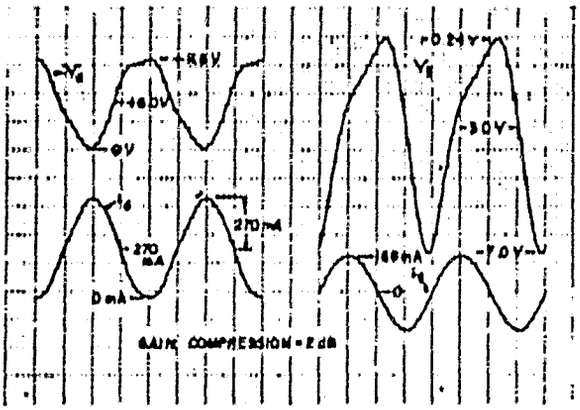

Fig. 5 Waveforms at V_d=+6.0 V, I_d= 270 mA, V_g=-3.0 V and 2 dB gain compression.

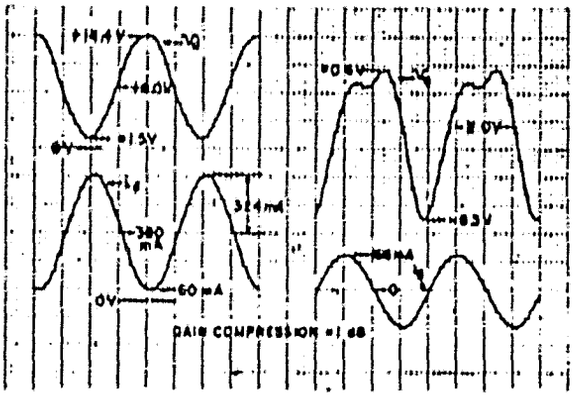

Fig. 6 Waveforms at V_d=+8.0 V, I_d= 380 mA, V_g=-2.0 V and 1 dB compression.

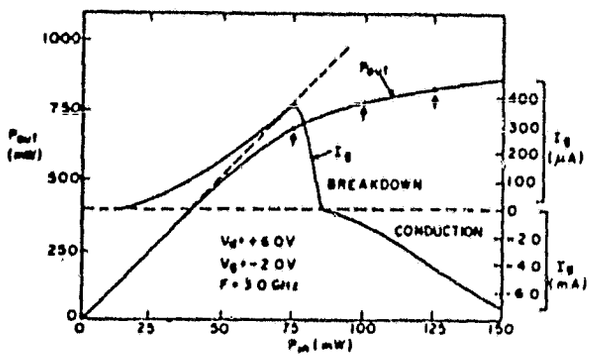

Fig. 7 Output power and DC gate current vs. input power.

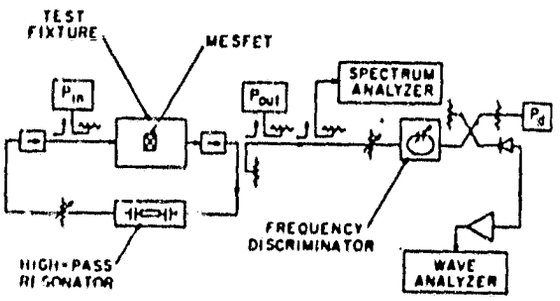

Fig. 8 Oscillator noise measurement setup.

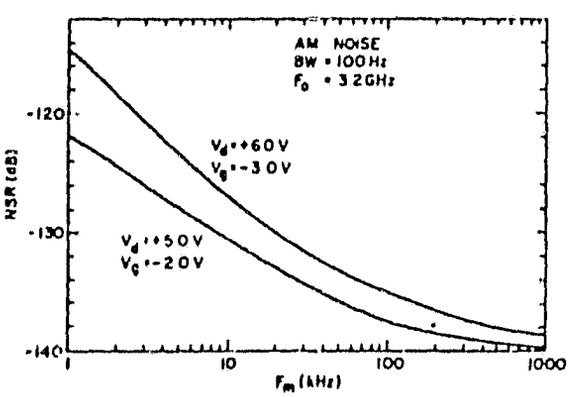

Fig. 9 Oscillator AM noise.

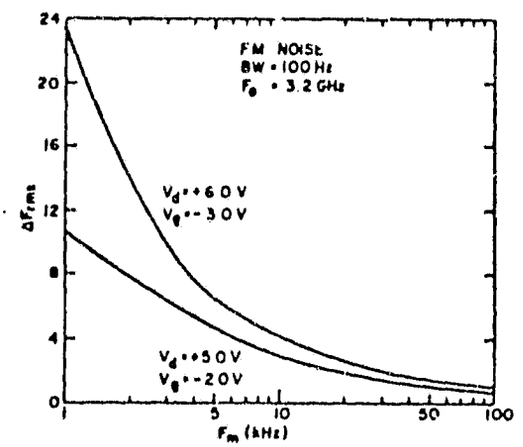

Fig. 10 Oscillator FM noise.

APPENDIX B

THEORY AND FABRICATION OF MESFETs

A. BASIC LARGE-SIGNAL MODEL

During the course of this program, we have refined and extended the large-signal analysis for the design of GaAs power FETs. Figure B-1 is a schematic diagram of the depletion region boundary under the gate for different gate voltages. With a small forward bias on the gate, the depletion region profile is similar to boundary 1 in Fig. B-1. The velocity is saturated at the drain end of the gate where the depletion depth is $(T - X_o)$. As the gate is reverse-biased and the reverse bias increases, the depletion boundary moves downward from profile 1 to profile 2 and so on until the channel pinches off. The dc bias on the gate puts the depletion layer boundary in the vicinity of profile 3. The rf swing moves the depletion boundary from profile 1 to pinch-off. Very little input power is dissipated in the channel in moving the boundary from 1 to 2. When the gate is biased by a superposition of dc and rf voltage, the depletion boundary moves sinusoidally with respect to profile 3. Hence, the charge under the gate also varies sinusoidally as:

$$Q = \frac{1}{2} Q_o \ (1 - \sin \omega t) \tag{1}$$

where $Q_o = neWX_o\ell_g$, n is free carrier density, W is channel width, ℓ_g is gate length, and X_o is active channel thickness. The input circuit current is

$$I_{in} = \frac{dQ}{dt} = -1/2 \ Q_o\omega \cos \omega t \tag{2}$$

The resistance of the channel through which the input current flows varies from a relatively low value in the forward bias portion of the cycle to a value approaching infinity at pinch-off. We can evaluate this resistance by noting that the channel is an RC tansmission line with the drain end open-circuited. The input impedance Z_t of an open-ended RC transmission line is given by

$$Z_t = Z_o/\text{Tanh}\left(\sqrt{j\omega R'C'L}\right) \tag{3}$$

where $Z_o = \sqrt{\frac{R'}{j\omega C'}}$

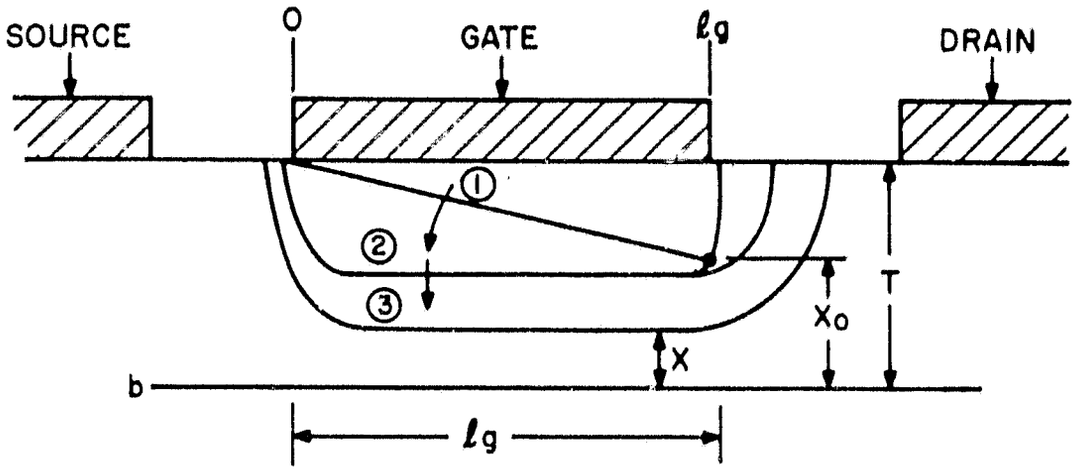

Figure B-1. Cross section of gate with various stages of carrier depletion of the channel.

R' and C' are the resistance and capacitance per unit length along the line, respectively. For typical FETs, $X_o T/\ell_g^2 > 0.01$ and the argument of the Tanh function is less than unity. Thus, we can approximate

$$Z_t = \frac{1}{3} R + \frac{1}{j\omega C} \tag{4}$$

where R and C are total channel resistance and total gate-channel capacitance, respectively. The effective channel series resistance is thus 1/3 the total channel resistance under the gate

$$R_{eff}(t) = 1/3\ R_{channel}(t) = 1/3\ \frac{\ell_g^2}{\mu Q_o} = \frac{2}{3}\left[\frac{\ell_g^2}{\mu Q_o}\right]\frac{1}{(1 - \sin \omega t)} \tag{5}$$

where μ is the electron drift mobility.

The average input power is given by

$$P_{in} = 1/T\int_{-T/2}^{T/2} I_{in}^2 R_{eff}(t)dt = \frac{1}{6}\frac{\omega^2}{\mu}\ell_g^2 Q_o \tag{6}$$

The spreading resistance from the source end of the channel increases the effective series resistance. We will account for this by using a multiplying factor Σ for Eq. (6)

$$\Sigma = (1 + \ell_s/\ell_g) \tag{7}$$

where ℓ_s is the source-gate separation.

The dc and rf I-V characteristics are as shown in Fig. B-2. The rf output current is given by

$$I_{out} = -\frac{1}{2}\frac{Q_o v_m}{\ell_g}\cos \omega t \tag{8}$$

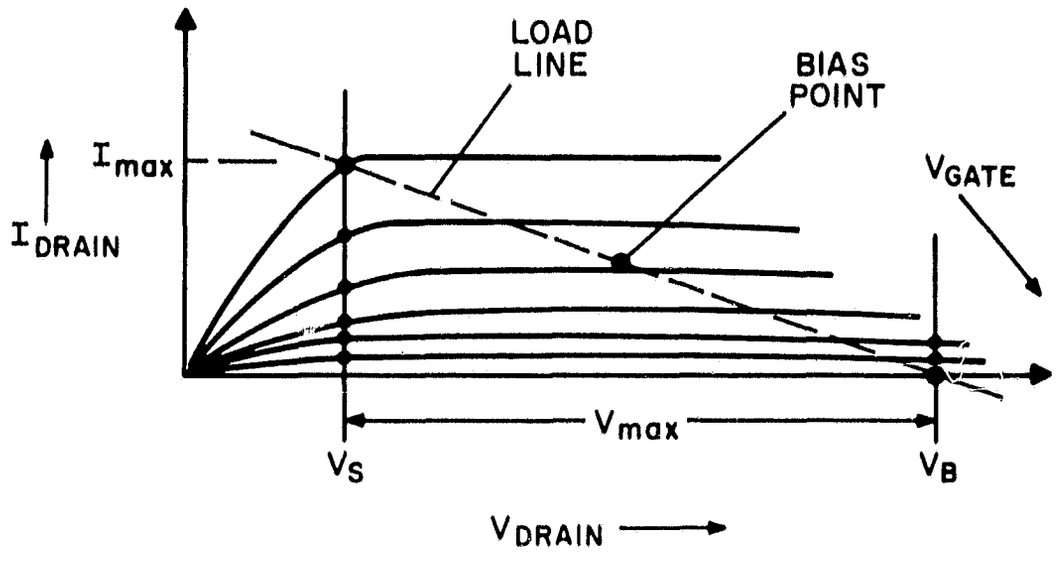

Figure B-2. I-V characteristic and load line of FET.

The rf output voltage is given by

$$V_{out} = \frac{1}{2} V_{max} \cos t \omega t \tag{9}$$

where v_m is maximum drift velocity, $V_{max} = (V_B - V_P - V_s)\rho$, V_B is breakdown voltage, V_P is pinch-off voltage, V_s is saturation voltage, and ρ is a phase shift degradation factor. The average output power is obtained from

$$P_{out} = \frac{-1}{T}\int_{-T/2}^{T/2} I_{out} V_{out} dt = \frac{1}{8} V_{max} Q_o v_m / \ell_g \tag{10}$$

A finite output conductance G_o absorbs some of the power supplied by the device. Treating G_o as a lossy shunt element across the load, the output power is reduced by a factor Γ:

$$\Gamma = 1 - \frac{G_o \ell_g}{Q_o v_m} V_{max} \tag{11}$$

For X-band GaAs FETs, Γ is on the order of 0.8.

The output power of the GaAs FET can be calculated from Eqs. (10) and (11). Notice that Q_o can be approximated by

$$Q_o = ne\ w\ T\ \ell_g \tag{12}$$

Therefore,

$$P_{out} = \frac{1}{8} V_{max}\ ne\ w\ T\ V_m\ \Gamma \tag{13}$$

The power gain is obtained from dividing the output power by the input power.

$$P_{out}/P_{in} = \frac{3}{4} \left[\frac{\mu v_m}{\omega^2 \ell_g^3}\right] V_{max} \frac{\Gamma}{\Sigma} \tag{14}$$

$\Gamma \leq 1$ and $\Sigma > 1$.

The maximum power gain increases with low-field mobility μ, maximum drift velocity v_m, breakdown voltage V_B, and is proportional to ℓ_g^{-3}. Γ and Σ can be calculated from Eqs. (11) and (7), respectively,

$$\Gamma = 0.81$$

and

$$\Sigma = 1 + \frac{0.3 \times 10^{-4}}{\ell_g}$$

Therefore, the power gain can be expressed as

$$\text{Power gain} = \frac{5.07 \times 10^3}{f^2 \ell_g^3 \left(1 + \frac{0.3}{\ell_g}\right)} \tag{15}$$

where f is in GHz, ℓ_g is in μm.

Equation (15) is plotted in Fig. B-3. The expected device gain is plotted as a function of frequency for various gate lengths. For a fixed gate length the gain drops off at 6 dB per octave increase of frequency, as expected. The measured G_{max} of RCA's 2.5-μm gate length GaAs power FETs is also shown. The theoretical calculations agree fairly well with our experimental results.

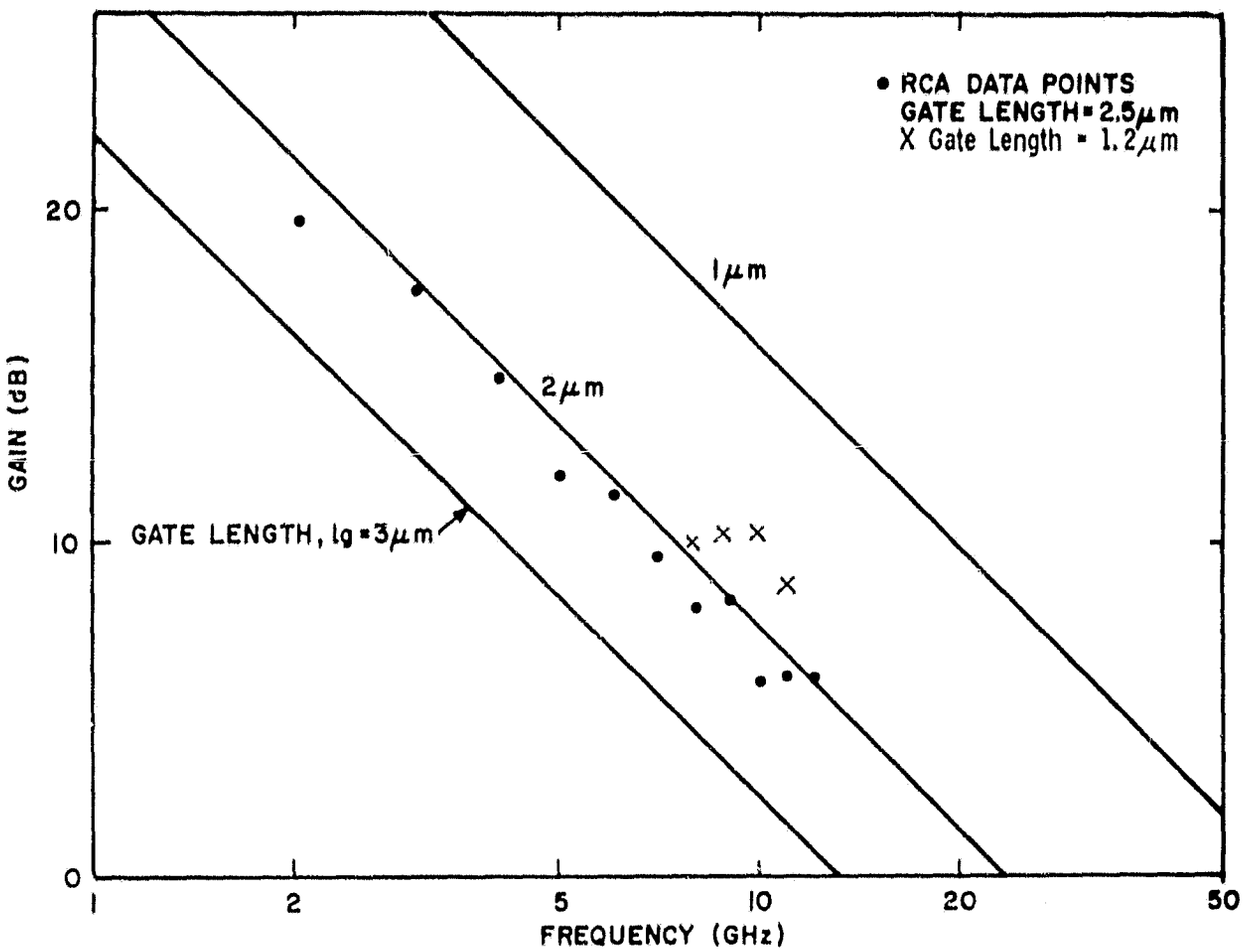

Figure B-3. Small-signal gain versus frequency with gate length as parameter.

Notice that the above calculation did not include the degradation factors such as gate width limitation, ohmic contact resistance, parasitic capacitance effects, and parasitic source inductance effects. These factors will be discussed in a later section. When these factors are taken into account, we find that devices with 150-μm gate width and 1-μm gate length will provide a useful gain of approximately 10 dB at 10 GHz.

B. DEVICE DESIGN

The basic large-signal model can be used to derive a set of design rules. These rules serve as a guideline for the choice of carrier concentration, layer thickness, gate length, and gate width. In order to keep these rules simple and to retain a proper physical insight, we will employ some approximations based on experimental results. The results of these design guidelines have been confirmed experimentally both at RCA and at other laboratories.

Given a set of performance requirements such as output power, gain, and operating frequency, the required gate length can be derived from Eq. (15). Since Eq. (15) did not take into account the degradation factors such as ohmic contact resistance, parasitic impedances, and material nonuniformity, we will assume that an intrinsic gain of 20 dB is required. We will further assume that the gate length is larger than 0.3 μm. Thus, we will neglect the $0.3/\ell_g$ term in Eq. (15). This assumption will introduce less than a 3-dB error in gain. The frequency range in which this model is valid is about 2 to 20 GHz. With the above assumption, Eq. (15) now becomes:

$$\ell_g = \frac{4}{f^{2/3}} \tag{16}$$

when ℓ_g is the required gate length in μm for the FET to have useful gain at f GHz. The required gate length is inversely proportional to $f^{2/3}$.

The required gate lengths for 4, 10, and 20 GHz operations are 1.4, 0.9, and 0.5 μm, respectively. Figure B-4 is a plot of ℓ_g as a function of frequency. The channel thickness T should be small compared with ℓ_g. If T is comparable to ℓ_g, the effective gate length will be much higher than the physical gate length ℓ_g as depicted in Fig. B-5. Assuming that the fringe field at the gate edge has a circular equipotential plane, and that the radius of the equipotential plane equals the depletion depth at the drain side plus one-half of the depletion depth at the source side (Fig. B-5), the effective gate length at the pinch-off condition is therefore:

$$\ell_{g\ effect} = \ell_g + 1.5\ T \tag{17}$$

If the channel thickness is equal to the physical gate length, $T = \ell_g$, the effective gate length is 2.5 times bigger than the physical gate length. It is desirable to keep T no bigger than 1/3 of ℓ_g. Assuming $\ell_g = 3T$, the channel

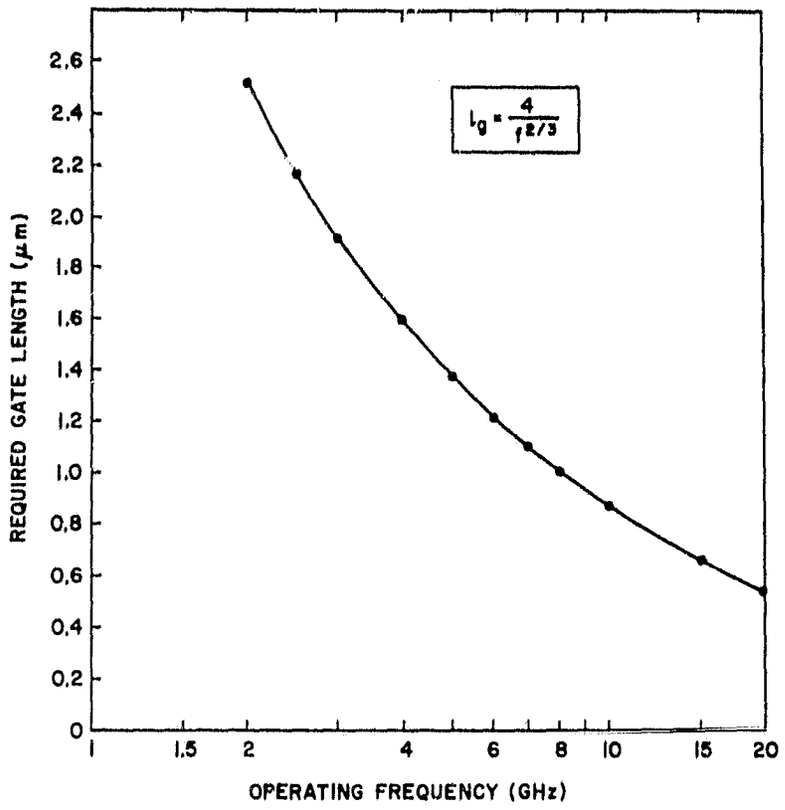

Figure B-4. Required gate length as a function of operating frequency.

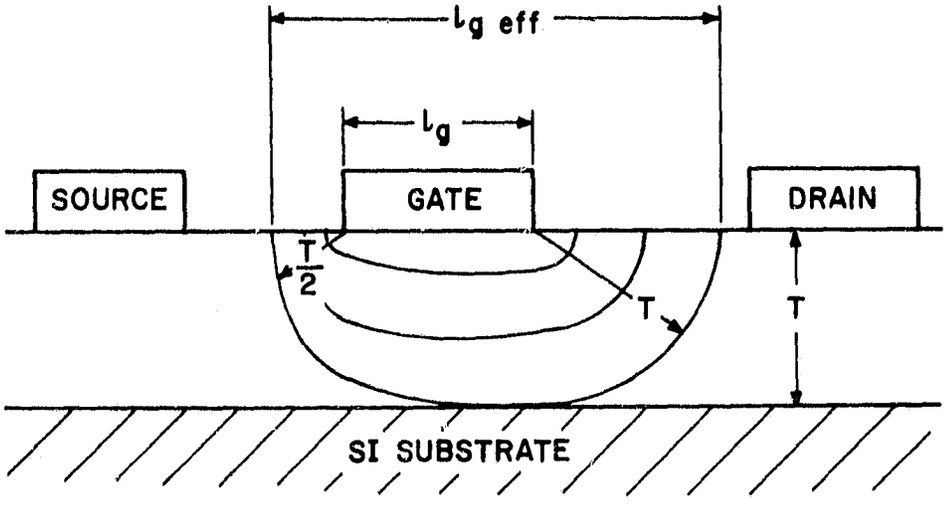

Figure B-5. Effective gate length of an FET. $\ell_{g\ eff} \cong \ell_g + 1.5\ T$.

thickness T can be calculated for each frequency. This is also plotted in Fig. B-4. The optimal nT product for power FETs is about 2.5×10^{12} cm^{-2}. Therefore, the carrier concentration n can be calculated. This is listed in Table B-1. With the carrier concentration n known, the bulk breakdown voltage V_B of the Schottky-barrier gate and the pinch-off voltage V_p can be calculated. V_B and V_P are also included in Table B-1. The instantaneous gate-to-drain voltage is roughly the sum of the dc drain bias voltage V_D, the gage bias voltage $|V_G|$, and the rf voltages on the drain and the gate. The dc gate bias voltage is roughly one-half the pinch-off voltage, $|V_G| = 1/2\ V_P$. The rf voltage is a function of the impedance matching at the gate and the drain side. Under certain matching conditions, the sum of the gate and drain rf voltages can be as high as the sum of the dc bias voltages [1]. For normal operating conditions, we can assume that the sum of the rf voltages is one-half the sum of the dc bias voltages. The maximum instantaneous voltage across the gate-drain terminal is:

$$|V_{gd}|_{max} = 1.5(V_D + |V_G|) \tag{18}$$

The dc gate bias voltage is usually set at one-half the pinch-off voltage V_P. In practical applications, where high reliability and long lifetime is required, it is desirable to keep $|V_{gd}|_{max}$ below the bulk breakdown voltage V_B. Substituting $|V_{gd}|_{max} = V_B$ and $|V_G| = 1/2\ V_P$, Eq. (18) becomes:

$$V_D = 0.67\ V_B - 0.5\ V_P \tag{19}$$

The dc drain bias voltage V_D as a function of frequency is also included in Table B-1. In actual device operation, the electric field in the channel is nonuniform and there is a voltage drop in the source-gate region. Therefore, the gate breakdown voltage is different from the bulk breakdown voltage V_B. The values listed in Table B-1 are, however, in reasonably good agreement with experimental observations. Hence, Table B-1 can serve as a semi-quantitative design guideline. Even with the ability of tailoring the channel thickness T

1. F. Sechi, H. Huang, and B. Perlman, "Voltage and Current Waveforms in Power MESFETs Operating at Microwave Frequencies," Digest, ISSCC 1978, San Francisco, CA, Session THPM 13.4.

TABLE B-1. GaAs FET DESIGN

$nT = 2.5 \times 10^{12} cm^{-2}$, $\ell_g = 3T$

Frequency, f (GHz)	?	4	8	10	15	20
Gate length, ℓ_g (μm)	2.52	1.59	1.0	0.86	0.66	0.54
n-layer thickness, T(μm)	0.84	0.53	0.33	0.29	0.22	0.18
Carrier concentrations, $n(cm^{-3})$	$3x10^{16}$	$4.7x10^{16}$	$7.6x10^{16}$	$8.6x10^{16}$	$1.1x10^{17}$	$1.4x10^{17}$
Schottky gate breakdown voltage V_B(V)	34	24	19	18	14	12
Pinch-off voltage V_p(V)	14	9	6	5.4	3.5	3
Estimated dc drain bias voltage V_D(V)	16	12	10	9	8	7

during device fabrication, the carrier concentration still needs to be controlled to within about 20% for a given frequency of operation. Because of the different carrier concentration profile at the n-layer/buffer layer interface with different reactors, the optimal value of n should be determined experimentally.

The pinch-off voltage of the FET is given by:

$$V_p = 1/2\ T^2 \frac{ne}{\varepsilon} = 1/2\ (nT)^2 \frac{e}{\varepsilon} \frac{1}{n} \text{ or } V_p \propto \frac{1}{n} \tag{20}$$

Since the nT product, or the operating current, is usually kept constant, the pinch-off voltage is inversely proportional to n. This can be seen from Table 4. The device designed for high frequency operation must have a lower pinch-off voltage than that designed for lower frequency.

The dc transconductance g_m is defined as:

$$g_m = \left| \frac{\Delta I_d}{\Delta V_G} \right| \tag{21}$$

Before the onset of velocity saturation, g_m is given by:

$$g_m = \left|\frac{\Delta I_d}{\Delta V_G}\right| \simeq \frac{ne\mu WT}{V_P} = \frac{2\varepsilon W}{nT}(n\mu) \tag{22}$$

where W is the total gate width. When the nT is kept constant, g_m is proportional to the product of the carrier mobility μ and carrier density n.

The output power per unit gate width can be calculated from Eq. (13) and Table B-1. For 10-GHz application, we have from Table B-1, T = 0.3 μm, n = 8.3×10^{16} cm^{-3}, V_B = 18 V, V_P = 5.4 V, V_D = 9 V. The maximum drain rf voltage (Fig. B-2) V_{max} can be calculated by the equation:

$$V_{max} = 2(V_D - V_S)$$

where V_S is the voltage at the onset of current saturation (Fig. B-2), $V_S \simeq$ 2 V. Hence, V_{max} = 14 V. Therefore, the output power per unit gate width is:

$$P = 1/8\ V_{max}\ neT\ V_m\Gamma = 5.6\ W/cm = 0.56\ W/mm$$

where $V_m = 10^7$ cm/s is the electron saturation velocity in GaAs and Γ = 0.8 is the degradation factor. We conclude that the power output is approximately 0.5 W/mm of gate width. The output power of a cell with four 150-μm gate stripes in parallel is therefore 300 mW. At 9 GHz, we have experimentally achieved an output power of 1 W from a 3-cell device. This corresponds to 0.56-mW/μm gate width. This is in fair agreement with theoretical calculations.

From the theoretical calculation and experimental results mentioned above, we conclude that the minimum gate widths required for cw 1-W and 4-W pellets are roughly 2000 μm and 8000 μm, respectively. Note that the gate width requirement is only one of the many important factors in device design. A device with a large gate width does not necessarily ensure high gain and high power output in X-band. Other factors such as device operating temperature, parasitic impedance, and phase incoherence can degrade both device output power and gain. We will now describe these factors in detail.

C. GaAs FET FABRICATION TECHNOLOGY

Our major objective in pursuing programs on GaAs FETs has been to develop a technology which leads to high performance-high reliability devices and which can be ultimately adapted to large-scale production. Our fabrication processes rely on conventional optical photoresists and make full use of self-aligned techniques. Modern microfabrication techniques such as ion-beam milling are used which avoid undercutting problems and result in almost a 1:1 photoresist pattern to actual device geometry ratio. We have also learned to use the material undercut which occurs during chemical etching to our advantage as exemplified by our self-aligned gate process.

Figure B-6 is a schematic cross section of a typical GaAs power FET. Figure B-7 is a scanning electron micrograph (SEM) showing a typical 8-gate FET pellet. The pellet size is 0.056 x 0.056 x 0.018 cm^3 (0.022 x 0.022 x 0.077 $in.^3$). Each cell consists of four 8-gate stripes in parallel. The gate length is nominally 1 μm and the gate stripe width is 150 μm corresponding to a cell source periphery of 1200 μm. Each cell has 5 sources and 4 drains.

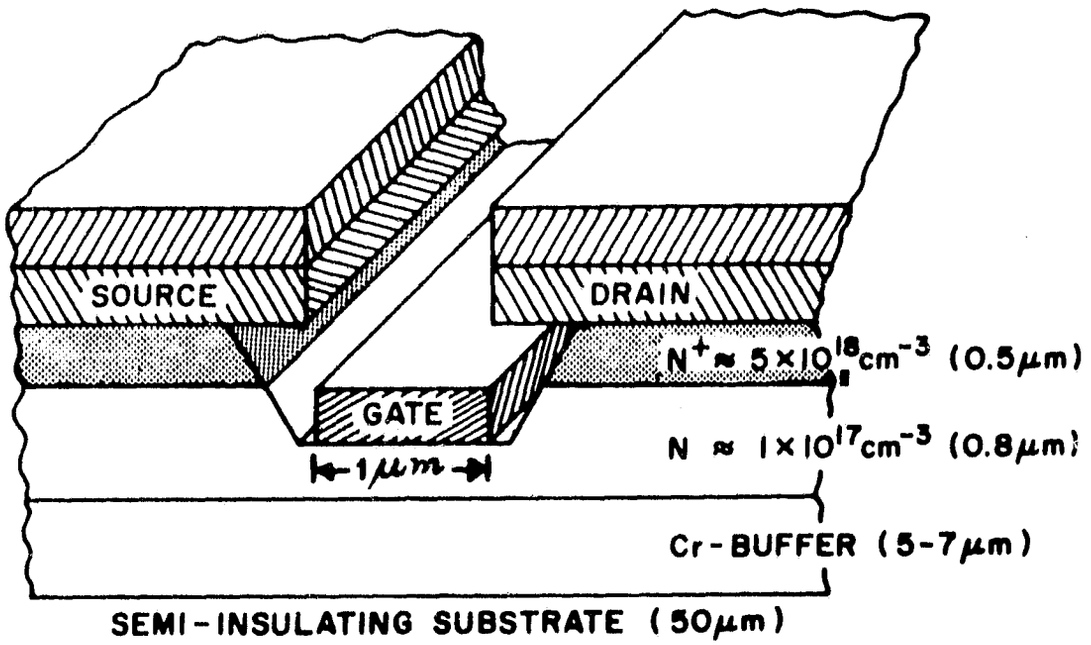

Figure B-6. Schematic cross section of RCA GaAs FET.

200X-45°

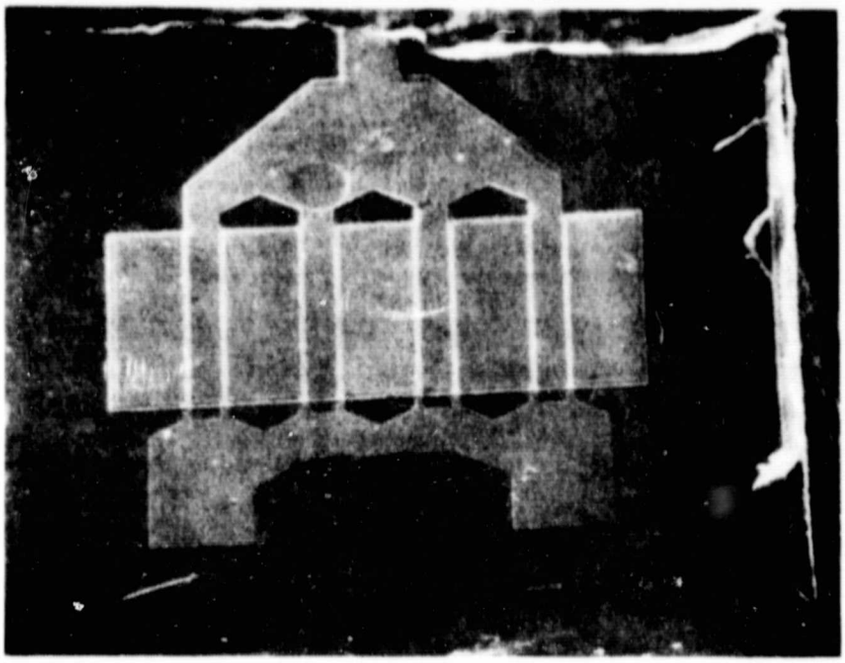

Figure B-7. An 8-gate FET pellet.

Device fabrication starts with an n^+-n-SI GaAs wafer grown as described previously. The wafer may or may not have a buffer layer. Since a buffer layer does not modify the fabrication process, we will ignore its presence in our description. This process can be described with reference to Fig. B-8. Conventional photolithographic techniques such as contact masking are used throughout. Standard positive working photoresists are used to define metallization patterns, and the metal itself is used to mask in order to form the channel and isolate the various device elements. The salient steps are:

(1) The source and drain areas are selectively metallized with AuGe/Ni ohmic contacts. The face is followed by a titanium-platinum and gold metallization.

(2) Photoresist patterning is used to define the mesa. Mesas are formed using ion-beam etching (IBE).

(3) A second photoresist pattern is defined which splits mesas into alternating source and drain electrodes. Openings (i.e., channels) in the photoresist between adjacent electrodes is about 1 μm.

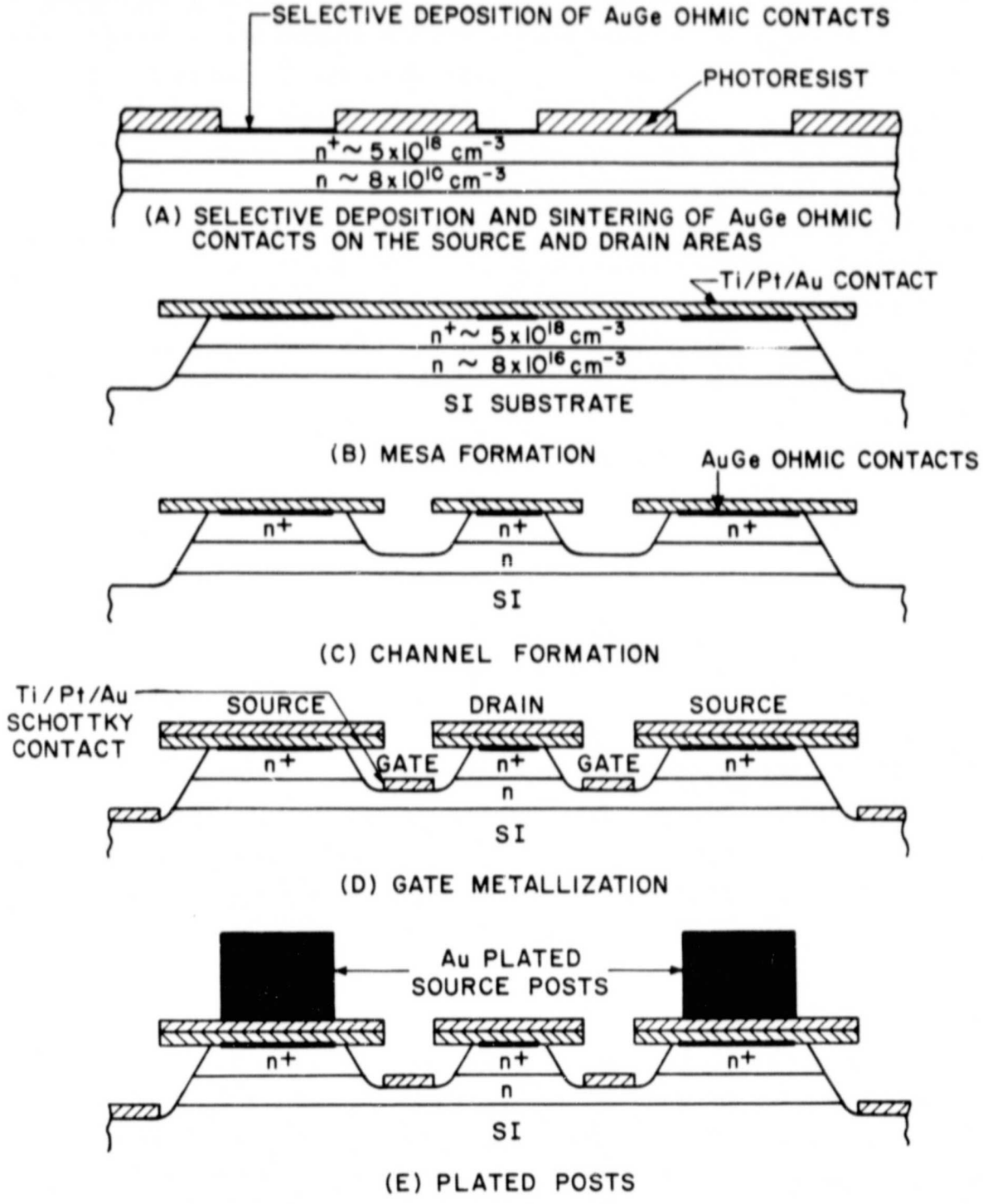

Figure B-8. Process diagram for the self-aligned gate process.

(4) The channels formed in the photoresist are cut using IBE down to the n-layer of the wafer. During IBE, source-to-drain saturation current (I_{DS}) is monitored and the process stopped when the channel thickness is appropriate for good FET performance. Typically, the value of I_{DS} at this point is 5 to 15 A/cm of gate width.

(5) A chemical "touch-up" etch is used to give enough undercut to prevent shorting in later steps (Fig. B-8).

(6) A second Ti/Pt/Au evaporation places the gate stripes into the channel formed by earlier steps. Since the source and drain pads are undercut, there is not shorting of gate to either pad. Also, because the material in the active channel is lightly doped ($\sim 10^{17}$ cm^{-3}), the titanium forms a Schottky-barrier contact (Fig. B-8d).

(7) Finally, a photoresist pattern is defined for the gate bonding pad. Excess metal is removed by IBE, and, after cleaning, devices are ready for dc testing.

The n^+-layer thickness of the wafer is carefully chosen to allow gate metallization thicknesses of between 4000 and 6000 Å. About 5000 Å of gate metallization is desirable to decrease the effects of gate metallization resistance. Excessive gate metallization can lead to short circuits between the gate and source or drain contacts.

The smallest gate length that can be achieved by this process is that set by the resolution of the photomask. Since ion-beam etching does not undercut, we can obtain 1:1 mask resolution to metal definition ratio. We have obtained excellent photomasks with 1-μm gate stripes and with these have obtained gate lengths just under 1 μm (Fig. B-9).

D. GaAs FET PACKAGING

It is necessary to ensure that FET mounting in a package or circuit is carried out without any added parasitic reactances in order to take full advantage of the intrinsic device capability. This is particularly true when high-performance X-band devices are required. It is also desirable to have a device package or carrier which enables one to characterize the

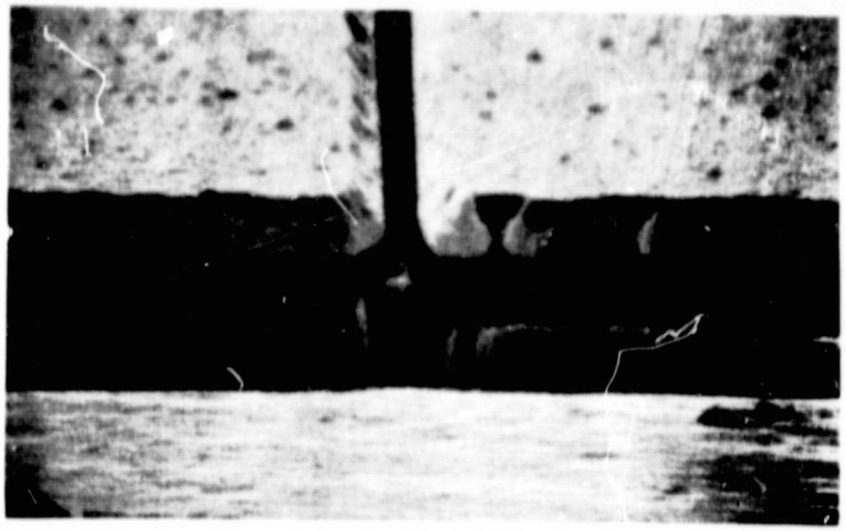

Figure B-9. SEM showing 0.5-μm gate length FET.

device on a network analyzer without having to commit it to any specific circuit. We have developed a carrier design which meets these objectives.

One of the parasitic reactances which degrade device performance in common source operation is the parasitic inductance from source to ground. In the device equivalent circuit, such parasitic inductance is equivalent to a resistance at the device input which degrades both available gain and noise figure. To provide low source-to-ground inductance it is important that the source contacts be as close to the rf ground as possible. We have developed a technique for flip-chip bonding the FET sources to a carrier which forms the rf ground plane. Our experimental results show that flip-chip mounting results in a 2- to 3-dB increase in the maximum available gain (MAG). An additional advantage of flip-chip mounting is that the device thermal resistance is decreased, leading to lowered junction temperature and improved reliability.

The source and drain contacts of our GaAs FETs are on the same level. In order to flip-chip bond the FET pellet, it is necessary to raise the source pad in elevation with respect to the drain pad. This is accomplished by plating up 15-μm-thick posts on the source pads. During this program period, we have developed the technology for plating posts.

Once the source pads are raised in elevation, wires or ribbons are bonded onto the gate and drain pads. For I- and J-band devices, wide, low inductance Au ribbons are used. Gold ribbons are bonded to the gate and drain pads. The pellet is flip-chipped onto the pedestal of a carrier by thermocompression bonding. The flying gate and drain leads are then bonded.

Figure B-10 is a photograph of two FETs flip-chipped on the carrier. The carrier consists of a gold-plated OFHC copper base and two ceramic standoffs. The copper base has dimensions of 0.15 x 0.46 x 0.064 cm^3 (0.060 x 0.180 x 0.025 $in.^3$). The 0.064-cm-thick ceramic standoffs are metallized on both surfaces. Gold straps are bonded from the drain pad of the FET to one standoff and from the gate pad to the other standoff. After the GaAs chip is mounted on the carrier, any subsequent handling and wire bonding are done to the carrier without disturbing the FET. The flip-chip mounting of an FET pellet onto a carrier is easily accomplished by a flip-chip bonder (Kulicke & Soffa*, Model No. 578-2). By the use of a partially transparent prism, the operator can see both the top carrier surface and the FET pattern. Therefore, the FET source pads can be aligned to the carrier bonding surface to within a few-

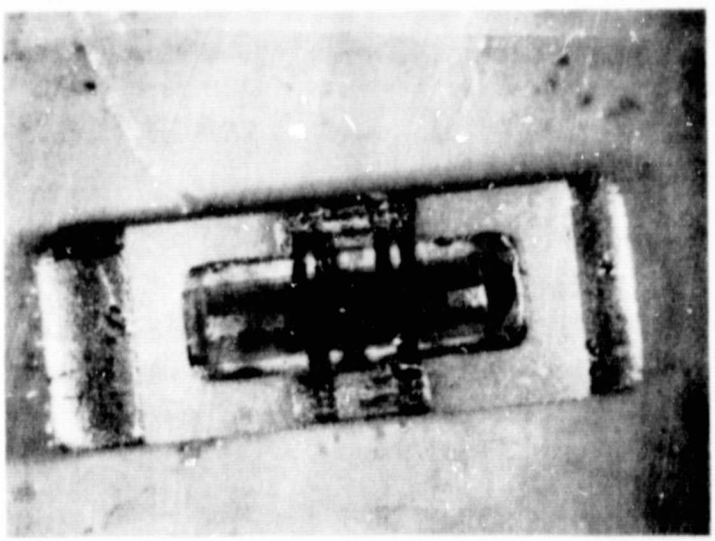

Figure B-10. Photograph of 2 FET pellets flip-chip mounted on a carrier.

*Kulicke and Soffa, Inc., Horsham, PA.

micrometer accuracy. Figure B-11 is a photograph taken from the flip-chip bonder's microscope. The FET pattern is aligned to the carrier bonding surface ready for flip-chip mounting. The gate and the drain ribbons are also aligned to the bond pads on the standoff.

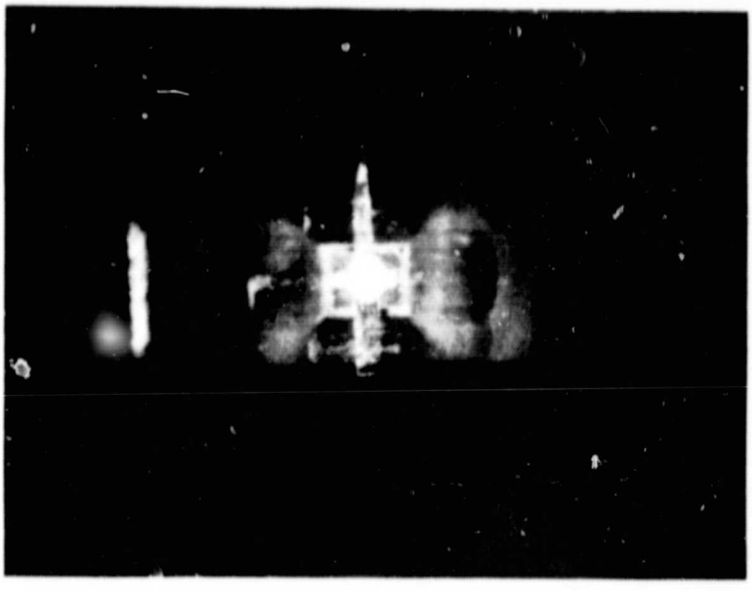

Figure B-11. Photograph taken from the flip-chip bonder's microscope. A 16-gate FET is aligned to the carrier ready for flip-chip mounting.

APPENDIX C

THERMAL CONSIDERATIONS IN FETs

One of the most important parameters in the design of a power FET is the maximum temperature rise in the channel. High operating temperature not only degrades the device performance but also greatly reduces the reliability of the device. It is crucial that the device thermal resistance be kept as small as possible. Since the thermal conductivity of GaAs is only 0.3 W/cm-°C while that of copper is 4 W/cm-°C, it is highly desirable to remove the heat through a minimum amount of GaAs. A flip-chip package meets this goal. In a flip-chip mounted device, the thermal flux spreads into copper after only 4 to 6 μm of GaAs. By comparison, in an up-side mounted device, the thermal flux has to travel through about 100 μm of GaAs before it reaches a copper heat sink. In this section, we will compute the thermal resistance of our proposed 1-W, single-cell device for both up-side and flip-chip mounting.

a. *Up-side Mounting* - Figure C-1 is a schematic diagram showing the thermal flux pattern in an up-side mounted device. Since GaAs is very fragile, the minimum wafer thickness that can be handled without breakage is about 100 μm. Selective etching of the GaAs substrate down to a few micrometers and refill of this hole with metal is not desirable, since differential thermal expansion of the refilled substrate may cause the GaAs to crack. Therefore, we will assume that the thermal path length in GaAs is 100 μm for the up-side mounted case.

Referring to Fig. C-1, we divide the device thermal resistance into two parts. The first part is the thermal resistance of the 100-μm-thick layer of GaAs (Region I). The second part is the thermal resistance of the copper heat sink (Region II). The Region I configuration is similar to that of a low-mu triode. The thermal resistance in Region I can be obtained by replacing the capacitance of the low-mu triode by thermal conductance, and replacing the permittivity by thermal conductivity. The capacitance of a

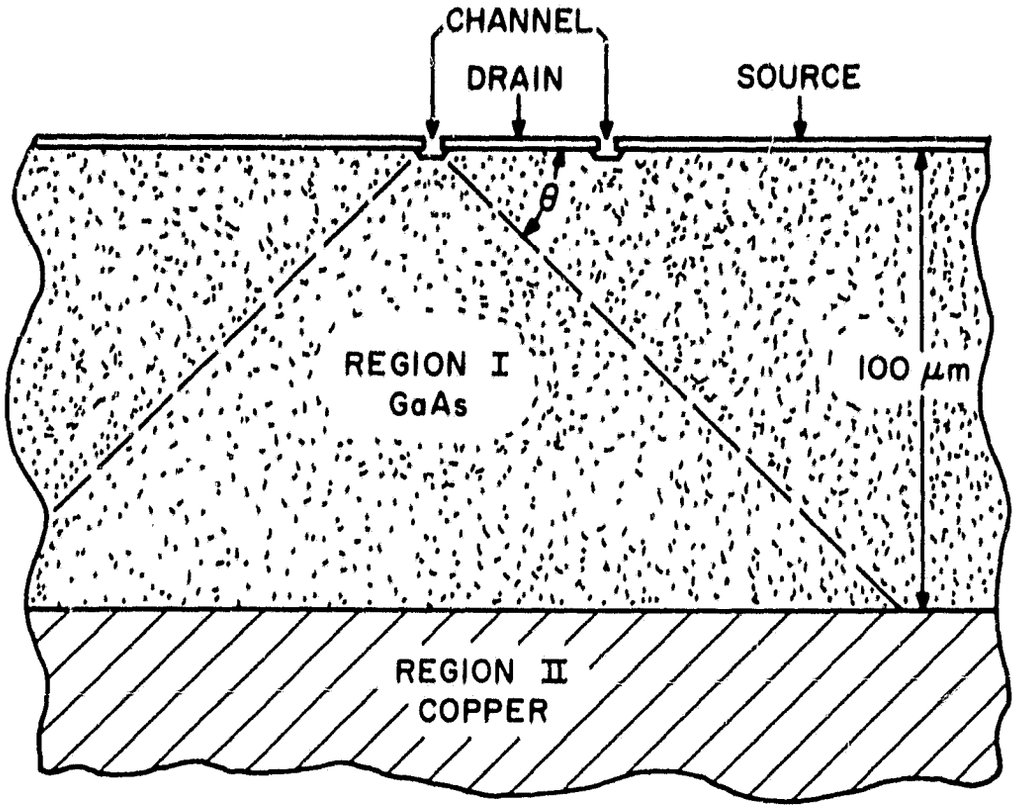

Figure C-1. Schematic diagram showing the thermal flux of an up-side mounted GaAs FET.

low-mu triode has been derived by Spangenberg [1]. By making appropriate substitutions, we can show that the Region I thermal resistance is:

$$R_{TH1} = \frac{1}{K_{GaAs}} \left[\frac{d_{gp}}{d} - \frac{1}{\pi} \ell_n \left(2 \sin \frac{0.125\pi \ell_g}{d} \right) \right] \frac{°C\text{-cm gate}}{W} \qquad (1)$$

where K_{GaAs} = 0.3 W/(°C-cm) is the GaAs thermal conductivity, d is the gate center-to-center separation, ℓ_g is the gate length, and d_{gp} = 100 μm is the thickness of the GaAs wafer. In our FET pattern, the gates are not uniformly

1. K. R. Spangenberg, *Vacuum Tubes* (McGraw-Hill Book Co., NY, 1948), pp. 125-130.

spaced. They were separated by alternate drain and source contacts. The drain contact is 23 μm long and the source contact is 51 μm long. For simplicity, we will assume a uniform spacing of 38 μm between the gates. Assuming a gate length of 1 μm, we can calculate the thermal resistance in Region I to be:

$$R_{TH1} = 12.88 \frac{°C\text{-cm gate width}}{W} \tag{2}$$

For the 1-W, single-cell pattern, the total gate width is 2400 μm. Thus, the thermal resistance in Region I is

$$R_{TH1} = 53.67\ °C/W \tag{3}$$

The thermal resistance in Region II can be calculated by assuming a uniform heat source on top of the copper heat sink. Assuming a 45° thermal spread angle in the 100-μm-thick GaAs, the area of the uniform heat source on copper heat sink is 350 x 636 μm. The thermal resistance of a rectangular heat source of dimensions ℓ x W on a semi-infinite heat sink can be expressed as:

$$R_{TH2} = \frac{1}{2K_{Cu}(\ell-W)} \ell_n \left(\frac{\ell}{W}\right) °C/W \tag{4}$$

In deriving the above expression a thermal spread of 45° is assumed. Using $K_{Cu} = 4$ W/(°C-cm), $\ell = 658$ μm, and $W = 350$ μm, we obtain

$$R_{TH2} = 1.1°C/W \tag{5}$$

Recall that the thermal resistance in Region I was 53.67°C/W. Thus, as expected, most of the thermal resistance of the device is contributed by the 100-μm-thick GaAs. The total thermal resistance for an up-side mounted FET is, therefore,

$$R_{TH,up} = \frac{1}{K_{GaAs}} \left[\frac{d_{gp}}{d} - \frac{1}{x} \ell_n \left(2 \sin \frac{0.125\pi\ell_g}{d}\right)\right] + \frac{1}{2K_{cu}(\ell-W)} \ell_n \left(\frac{\ell}{W}\right) °C/W \tag{6}$$

For a 1-W, up-side mounted FET, the total thermal resistance is

$$R_{TH,up} = 54.8°C/W \tag{7}$$

This is an optimistic estimate. The actual thermal resistance of the device is expected to be slightly higher.

It can be seen from Eq. (6) that the thermal resistance of an up-side mounted FET depends strongly on the GaAs thickness. Figure C-2 is a plot of calculated thermal resistance of a 16-gate (1-W) FET as a function of GaAs wafer thickness for different gate-to-gate separation. For a small gate-to-gate separation of 5 to 10 μm, the thermal resistance is about 80°C/W for a wafer thickness of 50 μm. Even the gate-to-gate spacing is in the 30- to 50-μm range; the wafer thickness has to be less than 30 μm to achieve a thermal resistance of 24°C/W to be compatible with the flip-chip case.

b. *Flip-Chip Mounting* - Figure C-3 is a schematic diagram showing the heat flow in a flip-chipped device. Heat is generated in the channel regions of the FET. It travels through only 6 μm of GaAs and reaches the plated source posts. The plated gold source post is 43 by 20 μm high. The drain stripe is 23 μm long. The channel length is approximately 1 μm. We divide the thermal resistance into four parts. Region I is GaAs; Region II are the source posts; Region III is part of the copper heat sink in which the thermal fluxes generated by each channel do not overlap; and Region IV is the remainder of the copper heat sink in which the thermal fluxes overlap.

In Region I, heat is generated in the channels and then travels through GaAs to the source posts. This configuration is equivalent to a pair of coplanar waveguides. The thermal conductance in Region I can be calculated by replacing the permittivity by the thermal conductivity, and capacitance by thermal conductance.

The capacitance of a coplanar waveguide has been derived by Wen [2]:

$$C = (\varepsilon_r + 1)\, \varepsilon_o \frac{2K(a/b)}{K'(a/b)} \tag{8}$$

2. C. P. Wen, "Coplanar-Waveguide Directional Couplers," IEEE Trans. on Microwave Theory and Techniques MTT-18, 318 (1970).

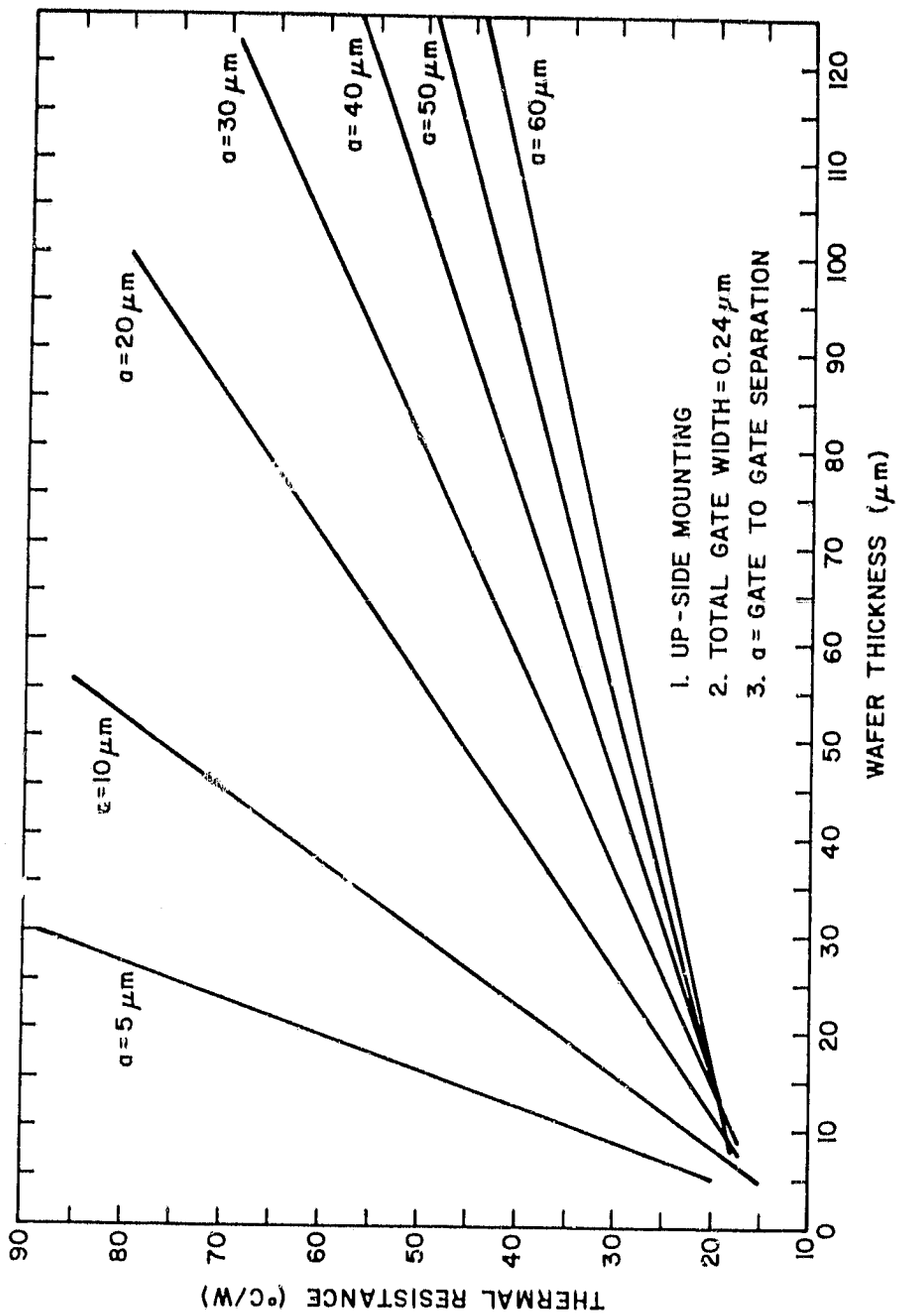

Figure C-2. Thermal resistance of a 16-gate FET mounted epi side up. The total gate width is 0.24 cm, designed for 1-W output power.

where ϵ is permittivity, K(k) is the complete elliptical integral of the first kind, $K'(k) = K(k')$, and $k' = (1 - k^2)^{1/2}$. The dimensions a and b are shown in Fig. C-3.

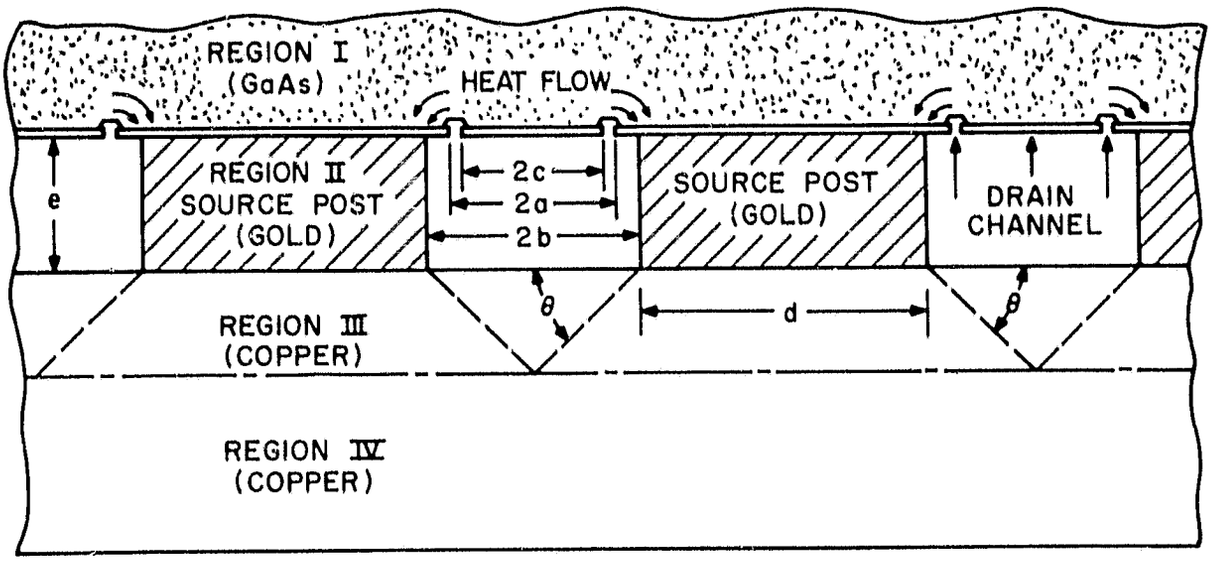

Figure C-3. Schematic diagram showing heat flow in flip-chipped GaAs FET. 2a = 25 μm, 2b = 41 μm, 2c = 23 μm, d = 35 μm, e = 20 μm.

For a drain contact (Fig. C-3) between two source posts, there is no heat flow and the contact temperature must be uniform. Therefore, we can treat the drain contact as the center conductor and the two adjacent source posts as ground planes. The thermal resistance in Region I is, therefore,

$$\overline{R}_{TH1} = \frac{1}{K_{GaAs}} \frac{K'(a/b)}{2K(a/b)} \frac{°C\text{-cm drain width}}{W} \qquad (9)$$

In the derivation of Eq. (9) from Eq. (8) the coefficient of the elliptic integrals has been reduced to $\epsilon_r \epsilon_o$ because there is no heat flow through air. In our case a/b = 0.61. Therefore, R_{TH1} can be calculated to be

$$\overline{R}_{TH1} = 1.88 \frac{°C\text{-cm drain width}}{W} \qquad (10)$$

Since the total gate width is 2400 μm and there are two gates per drain, the total drain width is 1200 μm. Hence, the thermal resistance in Region I is

$$\overline{R}_{TH1} = 15.68°C/W \tag{11}$$

Region II consists of 35- by 20-μm-high gold posts. The thermal conductivity of gold is $K_{Au} = 3.16$ W/(°C-cm). The thermal resistance per unit source width is given by

$$\overline{R}_{TH2} = \frac{e}{K_{Au}d} = \frac{20}{3.16x35} = 0.18 \frac{°C\text{-cm source width}}{W} \tag{12}$$

There are nine source posts, each 150 μm wide. The total source width is thus 1350 μm. Hence, the thermal resistance in Region II is

$$\overline{R}_{TH2} = 1.34°C/W \tag{13}$$

Region III is copper in which the thermal fluxes do not overlap and are thus independent. The contribution of Region III to device thermal resistance is very small. We will use an average length for estimation of R_{TH3}.

$$\overline{R}_{TH3} = \frac{b}{K_{Cu}(b+d)} = 0.12 \frac{°C\text{-cm source width}}{W} \tag{14}$$

so that the thermal resistance in Region III is:

$$\overline{R}_{TH3} = 0.86°C/W \tag{15}$$

Region IV is copper in which the thermal fluxes overlap. We assume a uniform heat source on a semi-infinite heat sink. The heat source is rectangular with a cross section of 636 x 177.5 μm. The thermal resistance in Region IV is thus given by

$$\overline{R}_{TH4} = \frac{1}{2K_{Cu}(\ell-W)} \ell_n \left(\frac{\ell}{W}\right) = 3.48°C/W \tag{16}$$

Adding Eqs. (11), (13), (15), and (16), we obtain the total thermal resistance for the flip-chip mounted, single-cell, 1-W pattern to be

$$\overline{R}_{TH\ Flip} = 21.05°C/W \tag{17}$$

Recall that the thermal resistance for the same 1-W pattern when up-side mounted is 54.8°C/W [Eq. (7)]. Therefore, the thermal resistance of an up-side mounted device is *more than twice* that of a flip-chip mounted device.

The temperature rise for a typical flip-chip, 1-W FET can be calculated. Assuming a device operating at 25% power-added efficiency with a 1-W output, 3 W are dissipated as heat in the FET. Temperature rise in the device is found from Eq. (10) as

$$\text{Temperature rise} = (21.05°C/W)\ (3\ W)$$
$$= 63.2°C$$

Therefore, the channel temperature of the 1-W FET is about 100°C. Recent reliability studies indicate a MTBF of 10^9 h for a low-noise FET operating at 80°C.

Figure C-4 shows the calculated thermal resistance of a 16-gate FET (2400-μm total gate width) as a function of gate-to-gate separation. When the gate-to-gate separation is less than 5 μm, the spreading thermal resistance becomes very large. Figure C-5 shows the relative contribution of thermal resistance from the GaAs and the metal for a 16-gate flip-chip FET. Even with 4-μm thermal path in GaAs, the thermal resistance of the GaAs part is still higher than that in the metal. In our FET pattern design, we have chosen the dimension such that the total temperature rise is less than 100°C above ambient to ensure reliable operation.

In the above discussion, we have chosen the 16-gate (2400-μm) FET as an example. The calculated thermal resistance of various types of flip-chip packaged FETs is summarized in Table C-1. The total gate widths range from 300 to 9600 μm and are designed for different power output. The thermal resistance of the FETs is roughly inversely proportional to the total gate width. Thus, the operating temperature is nearly constant regardless of the output power level. The designed operating temperature for all the FETs listed in Table C-1 was, in all cases, less than 100°C for a 20°C ambient. We feel that low operating temperature is an important factor to achieving high reliability operation. For satellite communications applications, an operating temperature of less than 110°C is highly desirable.

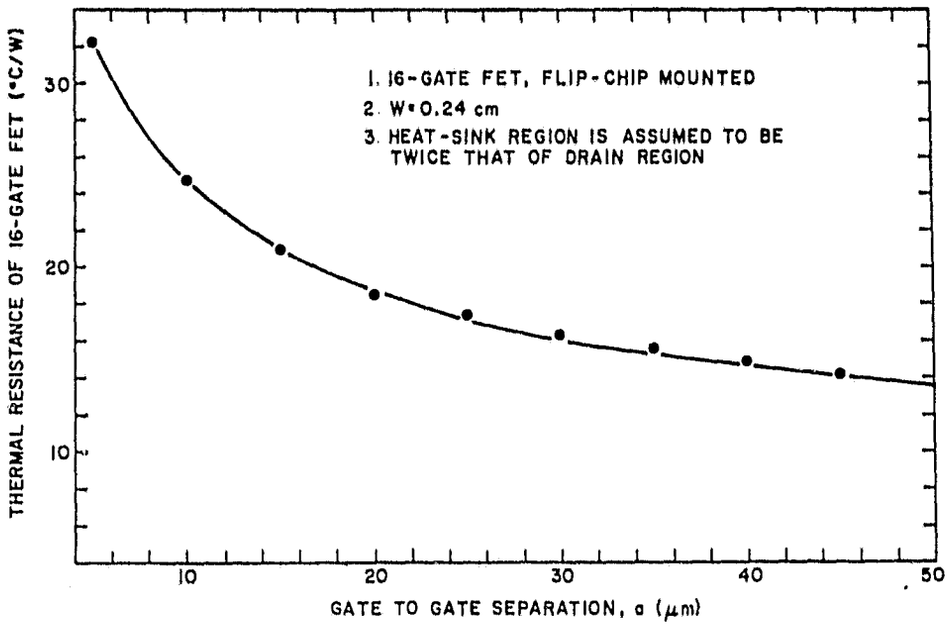

Figure C-4. Thermal resistance of a flip-chip mounted 16-gate GaAs FET as a function of gate-to-gate separation.

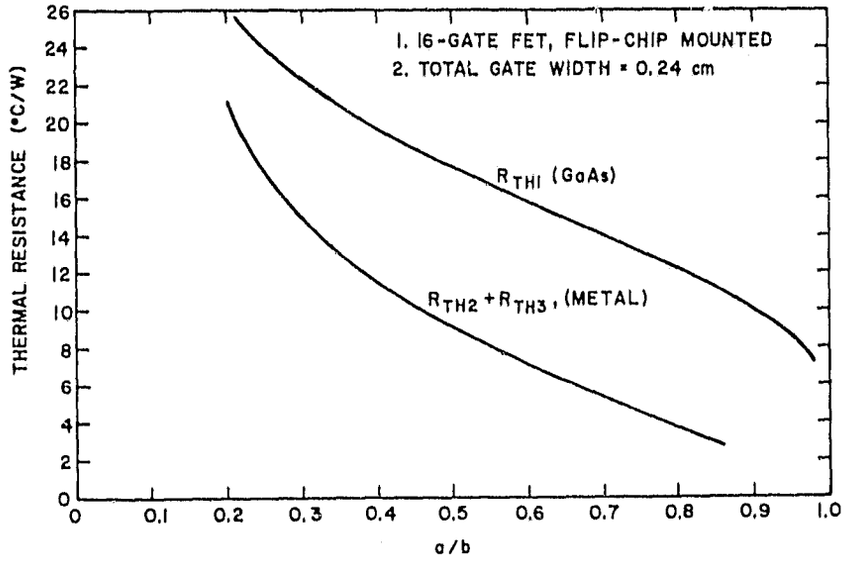

Figure C-5. Relative contribution of thermal resistance in GaAs and in heat sink as a function of heat-sink ratio a/b. Calculation is made for 16-gate FET, flip-chip mounted; total thermal resistance is the sum of the two curves.

TABLE C-1. FET THERMAL RESISTANCE

Designation	2G	4G	8G	16G	32G	48G
Gate Stripes per Cell	2	4	8	16	32	200
Gate Stripe Width (μm)	150	150	150	150	150	200
Gate Width per Cell (μm)	300	600	1200	2400	4800	9600
No. of Cells per Pellet	1	5	1	1	1	1
Drain Contact Width (μm)	25	25	25	12	12	12
Source Post Width (μm)	50	50	50	30	30	30
Design Output Power (μm)	0.15	0.25	0.5	1.0	2.0	4.0
Calculated Flip-Chip Cell Thermal Resistance (°ε/W)	168	84	42	21	11	6